A 1.4V Signal Swing Hybrid CLS-Opamp/ZCBC Pipelined ADC Using a 300mV Output Swing Opamp

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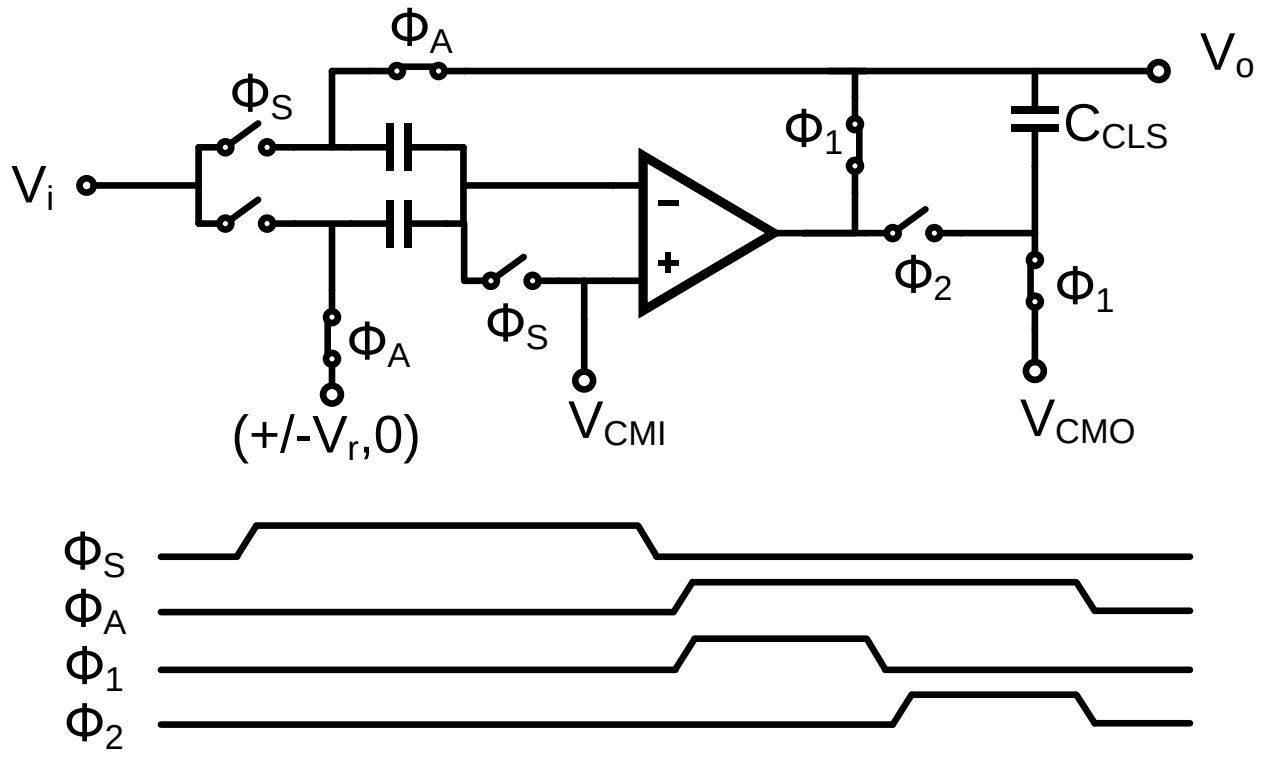
Preview

1. Background
   - Correlated Level Shifting
   - Zero-Crossing Based Circuits
2. Hybrid CLS-Opamp/ZCBC Structure
3. Dynamic Zero-Crossing Detector
4. Measurement Results

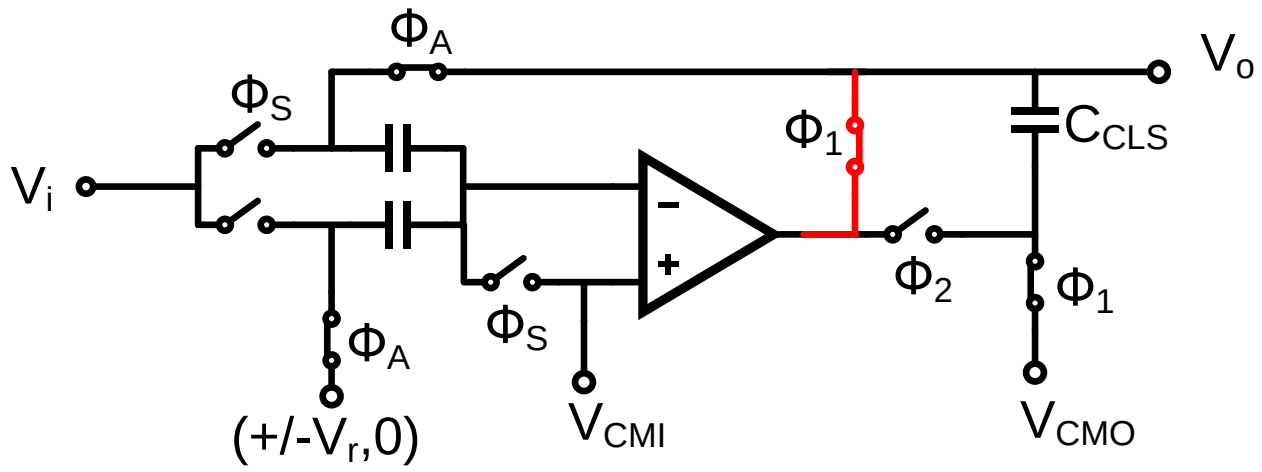
Correlated Level Shifting (CLS)



- Finite opamp gain error becomes $1/A^2$
- Opamp output tied to different nodes in Φ_1 and Φ_2

Gregoire, ISSCC 2008

CLS – Basic Operation



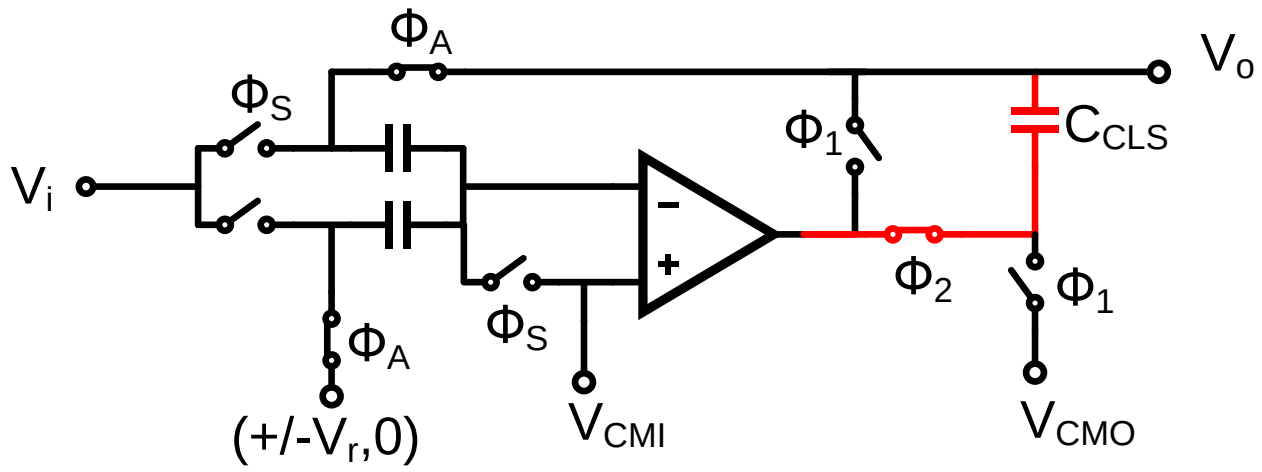
Φ_1 :

- opamp charges output directly
- processes full signal

Opamp Design Requirements

	Φ_1	Φ_2
Output Swing	**Large**	**Small**
Slew Rate	**Large**	**Small**

CLS – Basic Operation



Φ_2 :

- opamp is level shifted to mid-rail
- processes error only

Opamp Design Requirements

	Φ_1	Φ_2
Output Swing	**Large**	**Small**
Slew Rate	**Large**	**Small**

Observation

- Use separate charging devices for Φ_1 and Φ_2
- Optimized design for each phase
  - Increase overall accuracy & efficiency
- For this test chip:
  - Φ_1: Zero-crossing based circuit (ZCBC)
  - Φ_2: Double-cascoded telescopic opamp

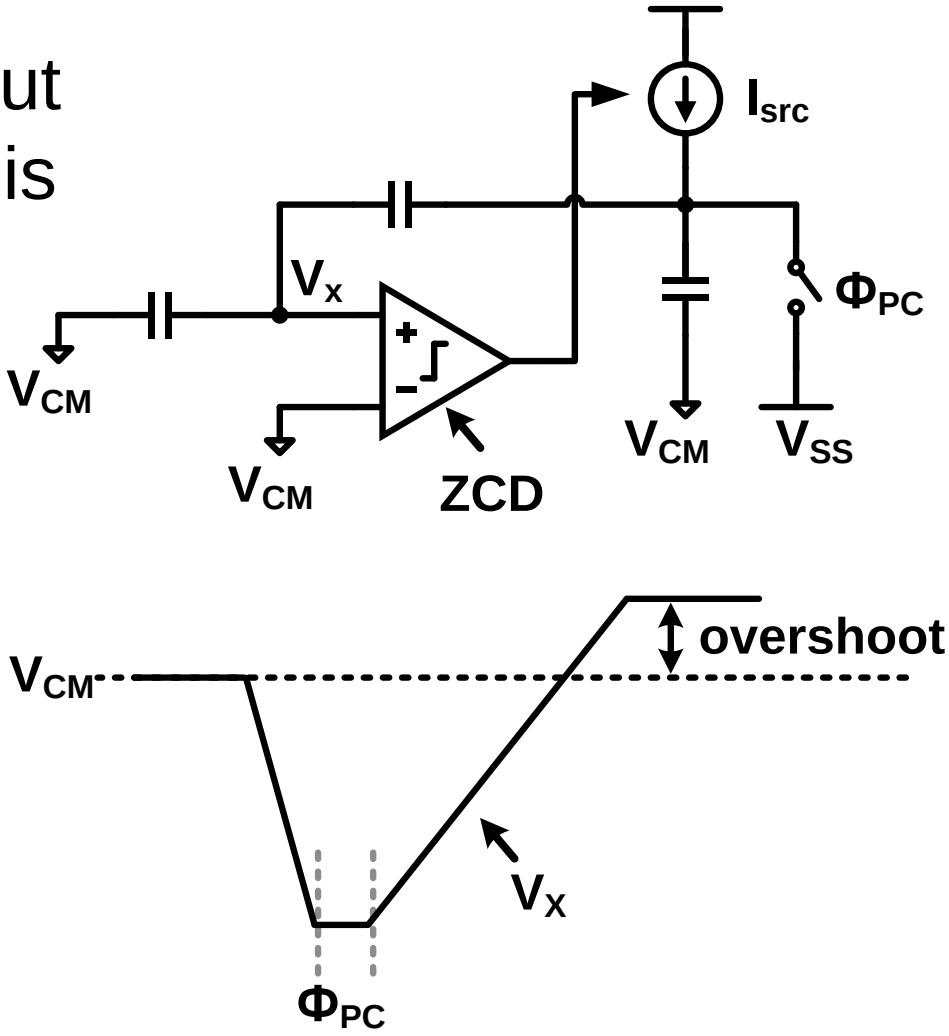
Opamp Design Requirements

	Φ_1	**Φ_2**
Output Swing	**Large**	**Small**
Slew Rate	**Large**	**Small**

Φ_1: Zero-crossing based circuit

Charges output until input virtual ground condition is detected

- \+ Slewing efficiency
- \+ Easy to turn off during Φ_2
- – No forced feedback
- – Linearity and reliability challenges



Sepke, ISSCC 2006

Φ_1: Zero-crossing based circuit

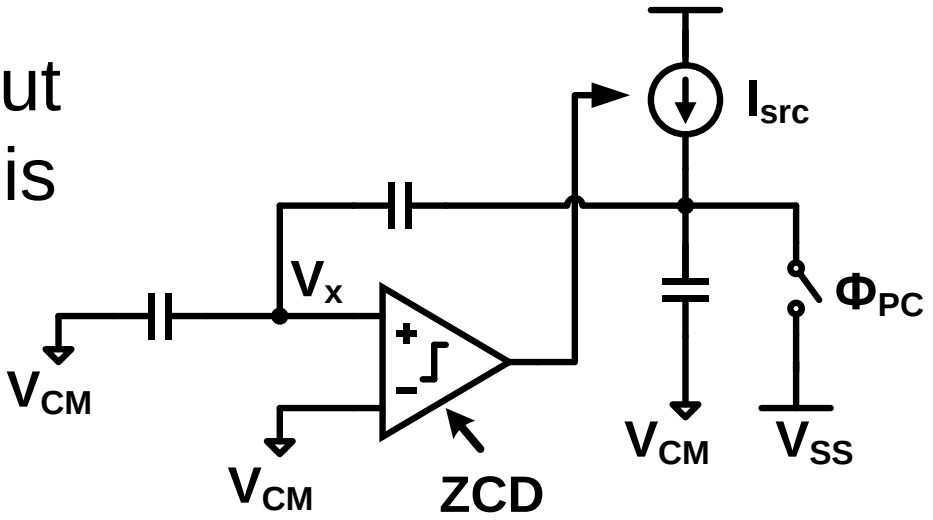
Charges output until input virtual ground condition is detected

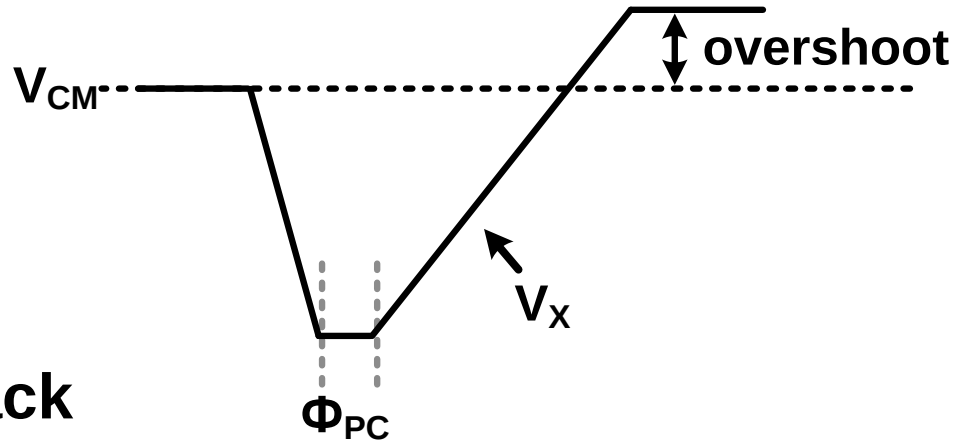
- \+ Slewing efficiency
- \+ Easy to turn off during Φ_2

- ✓ No forced feedback
- ✓ Linearity and reliability challenges

Φ_1 : Fast, coarse charging

Φ_2 : High accuracy feedback

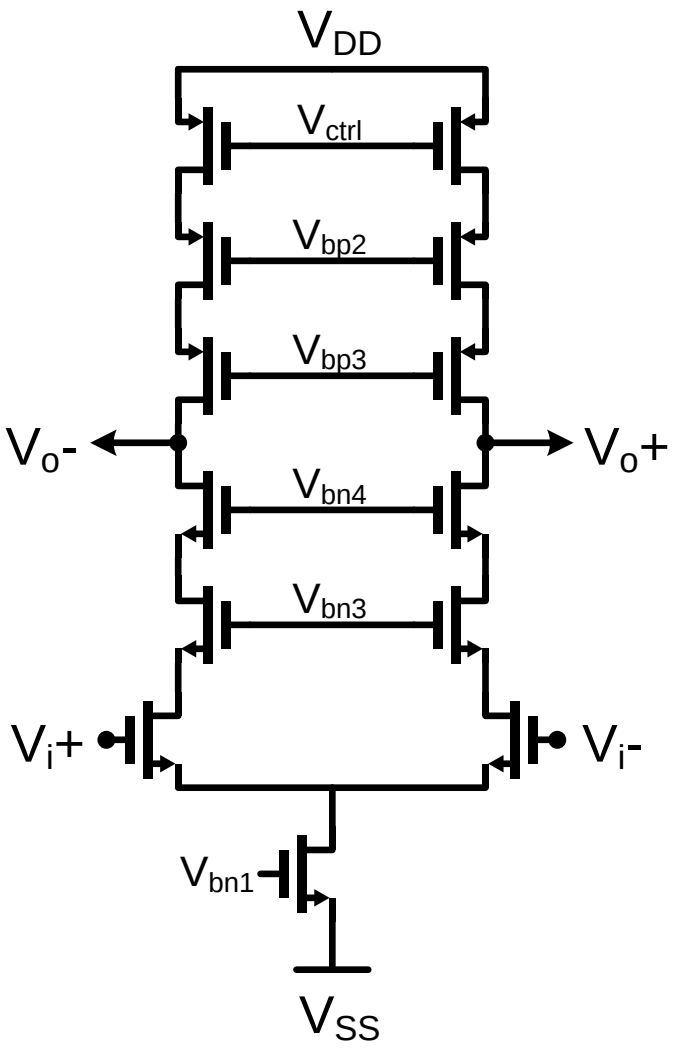




Sepke, ISSCC 2006

Φ_2: Telescopic Opamp

- \+ High Gain
- \+ High Speed
- \+ Low Power
- – Low Swing
- – Low Slew



Φ_2: Telescopic Opamp

- \+ High Gain
- \+ High Speed
- \+ Low Power
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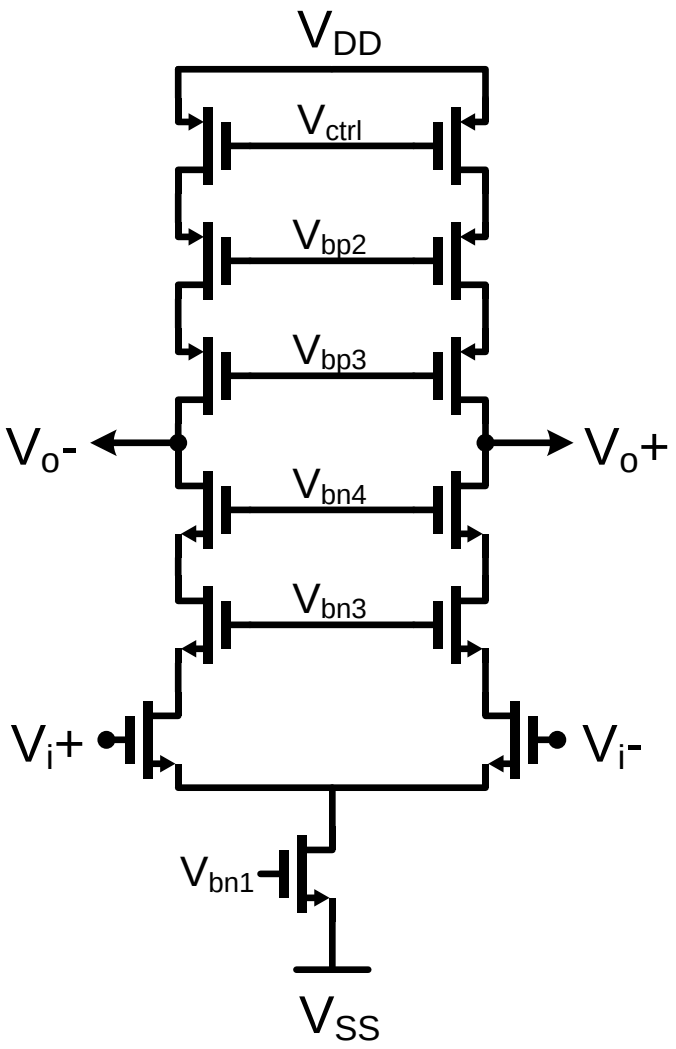
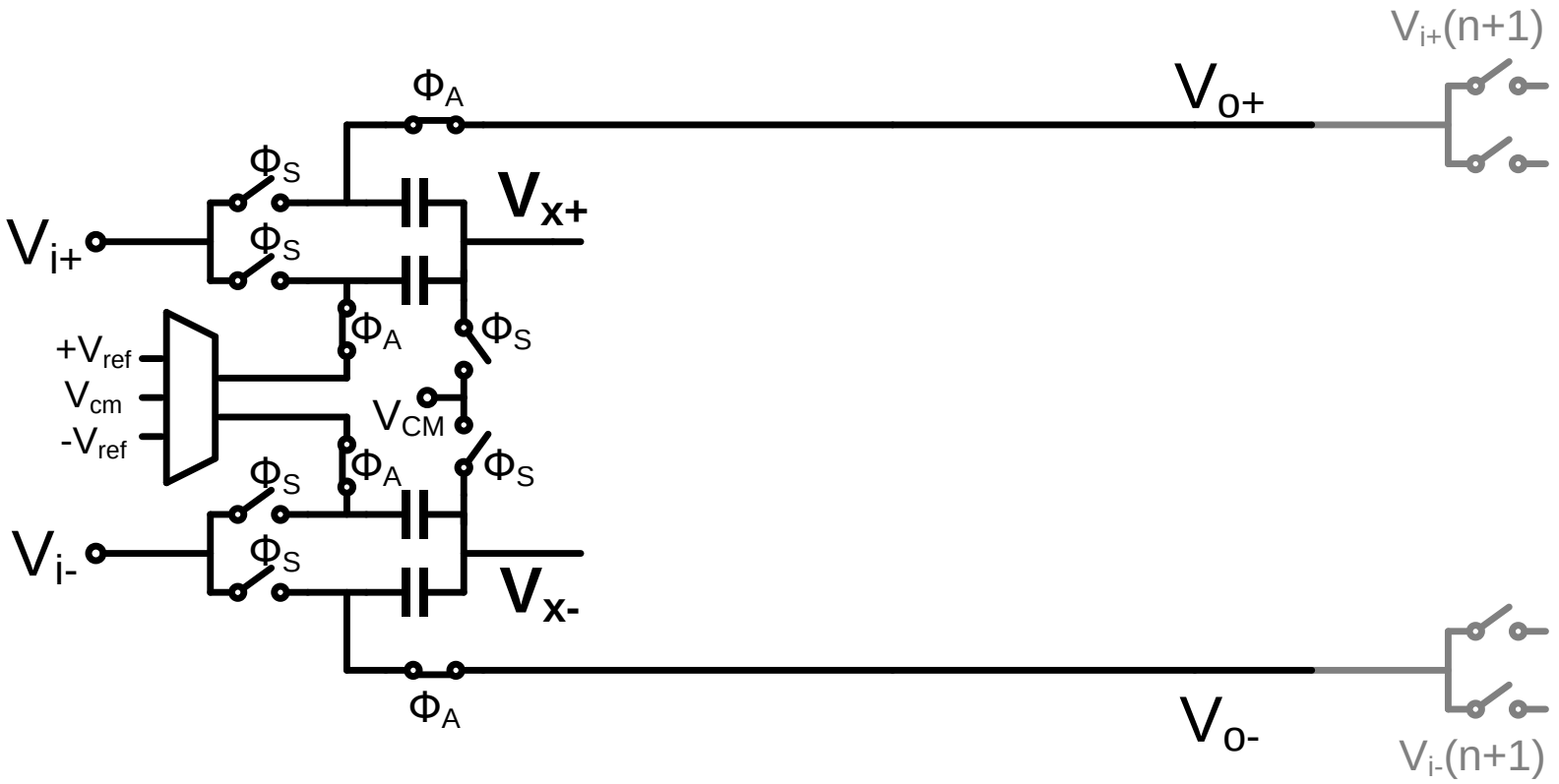


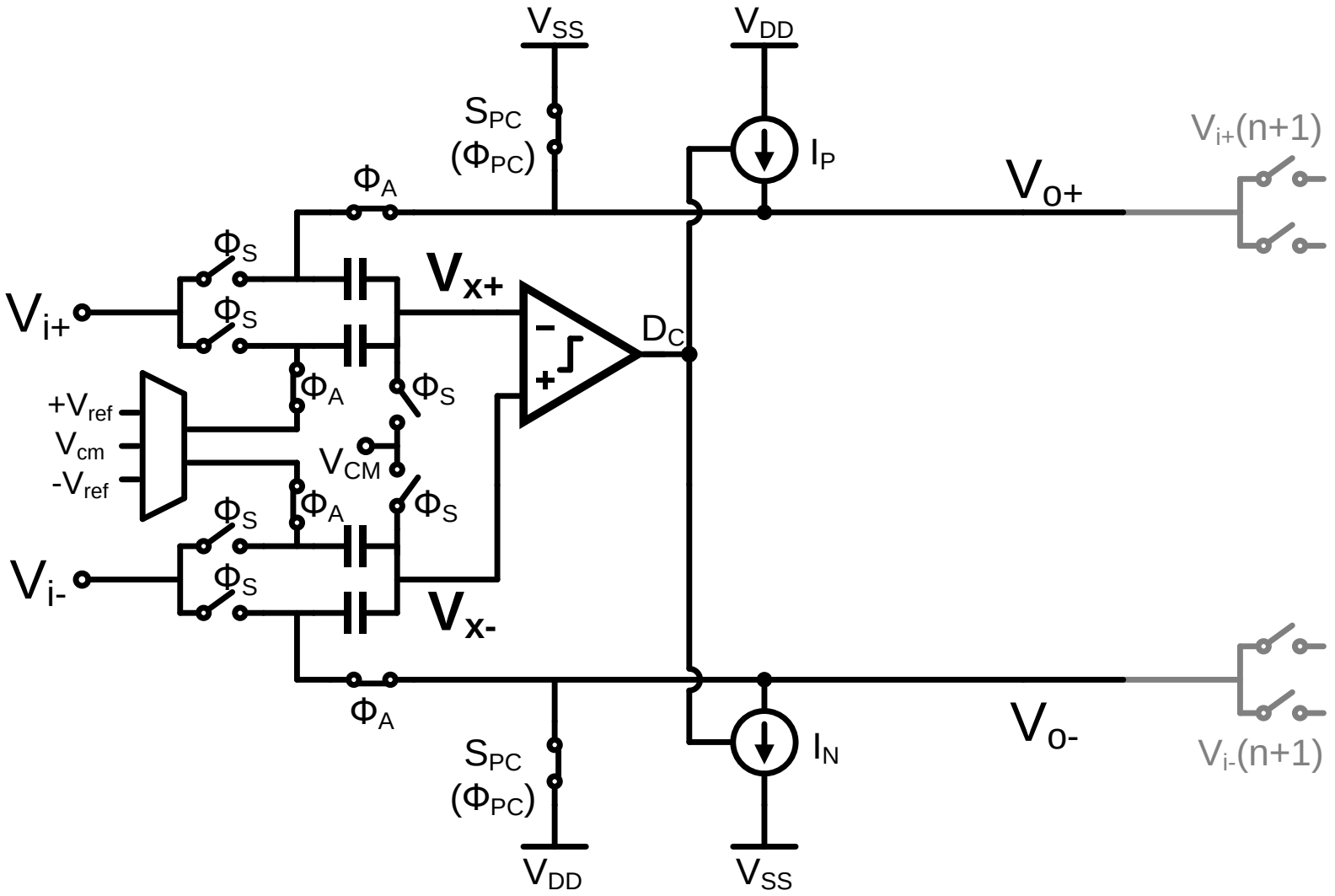
Effective Gain

35dB ($A_{\Phi 1}$)
+ 75dB ($A_{\Phi 2}$)
110 dB

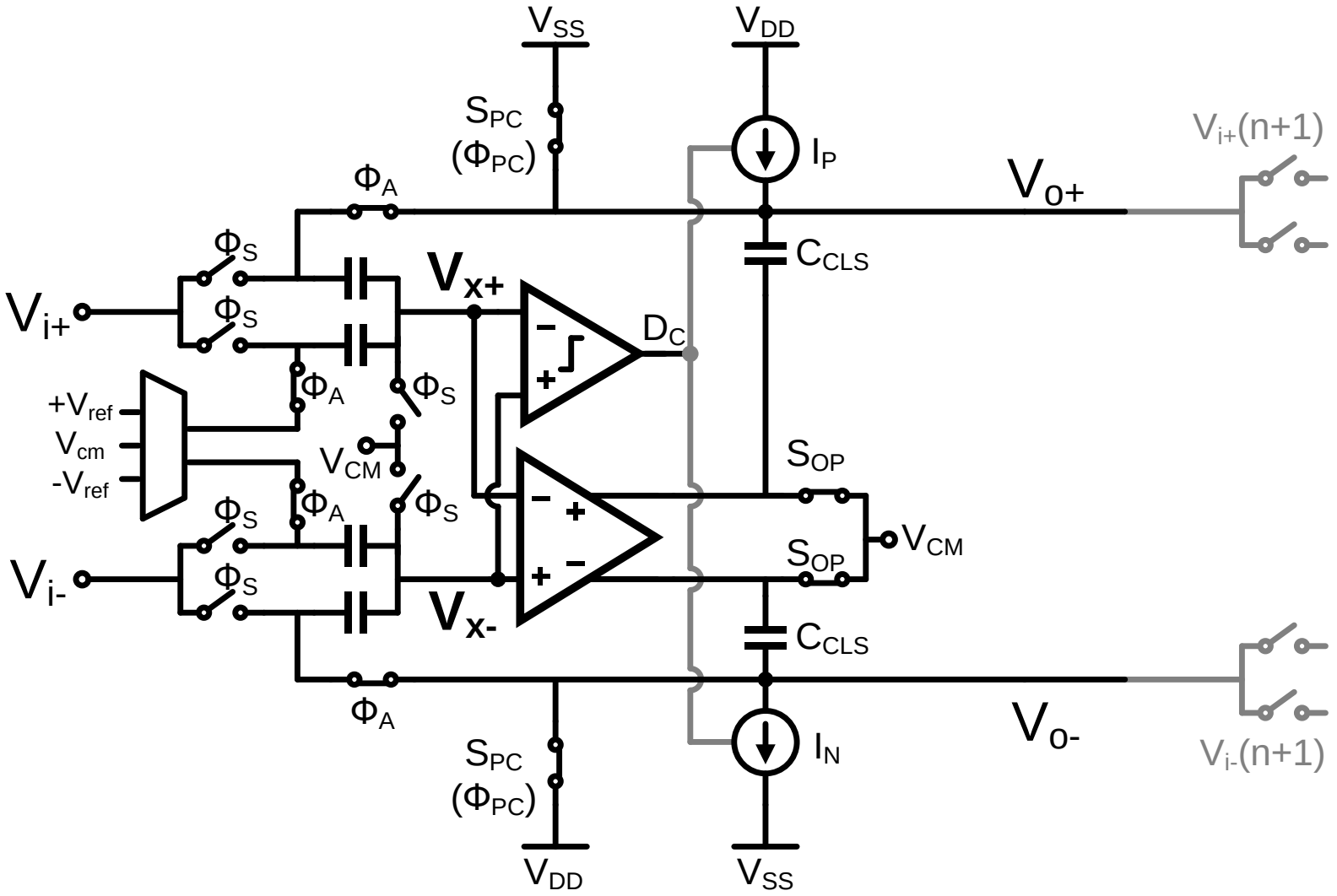
Hybrid CLS-Opamp/ZCBC



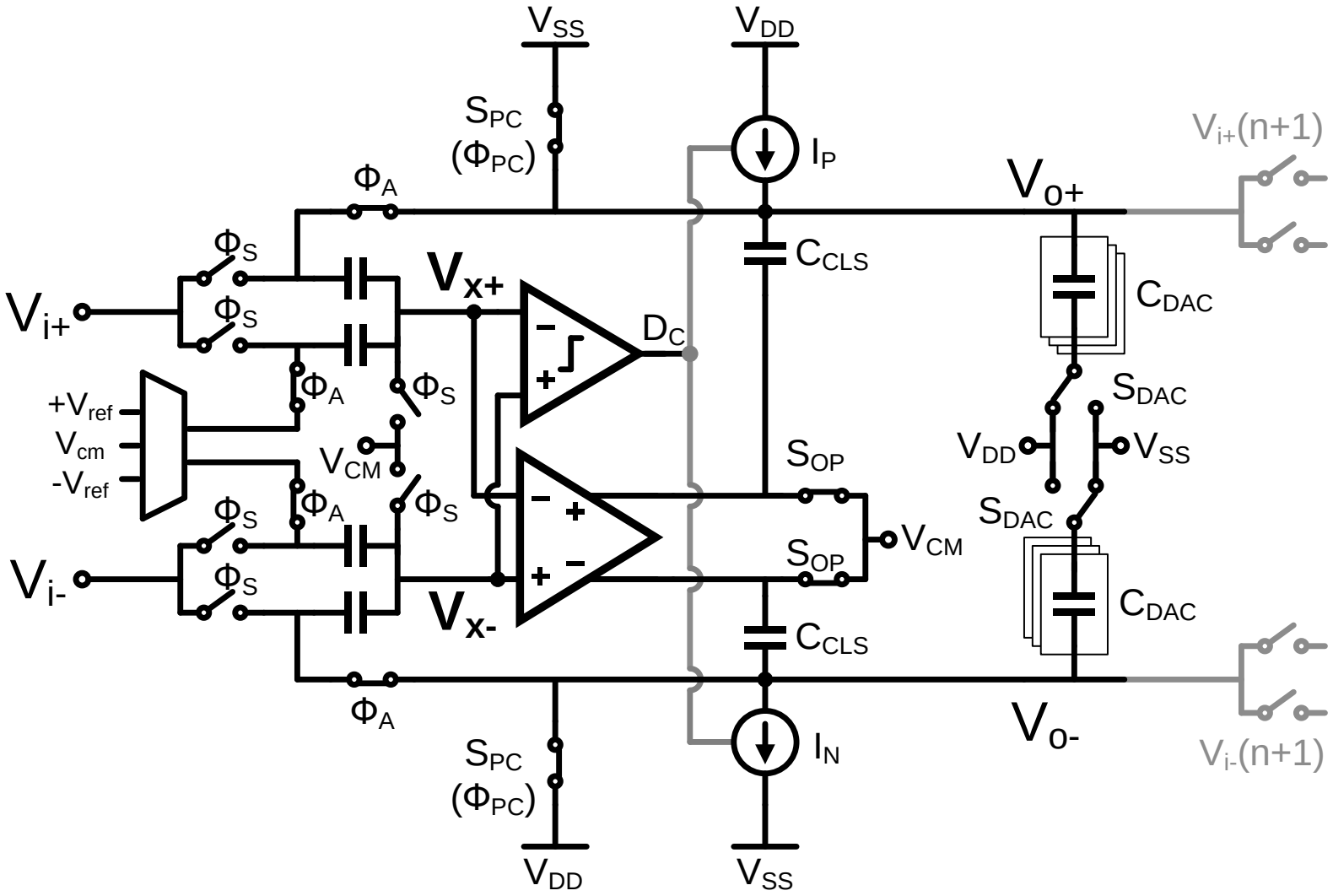
Hybrid CLS-Opamp/ZCBC

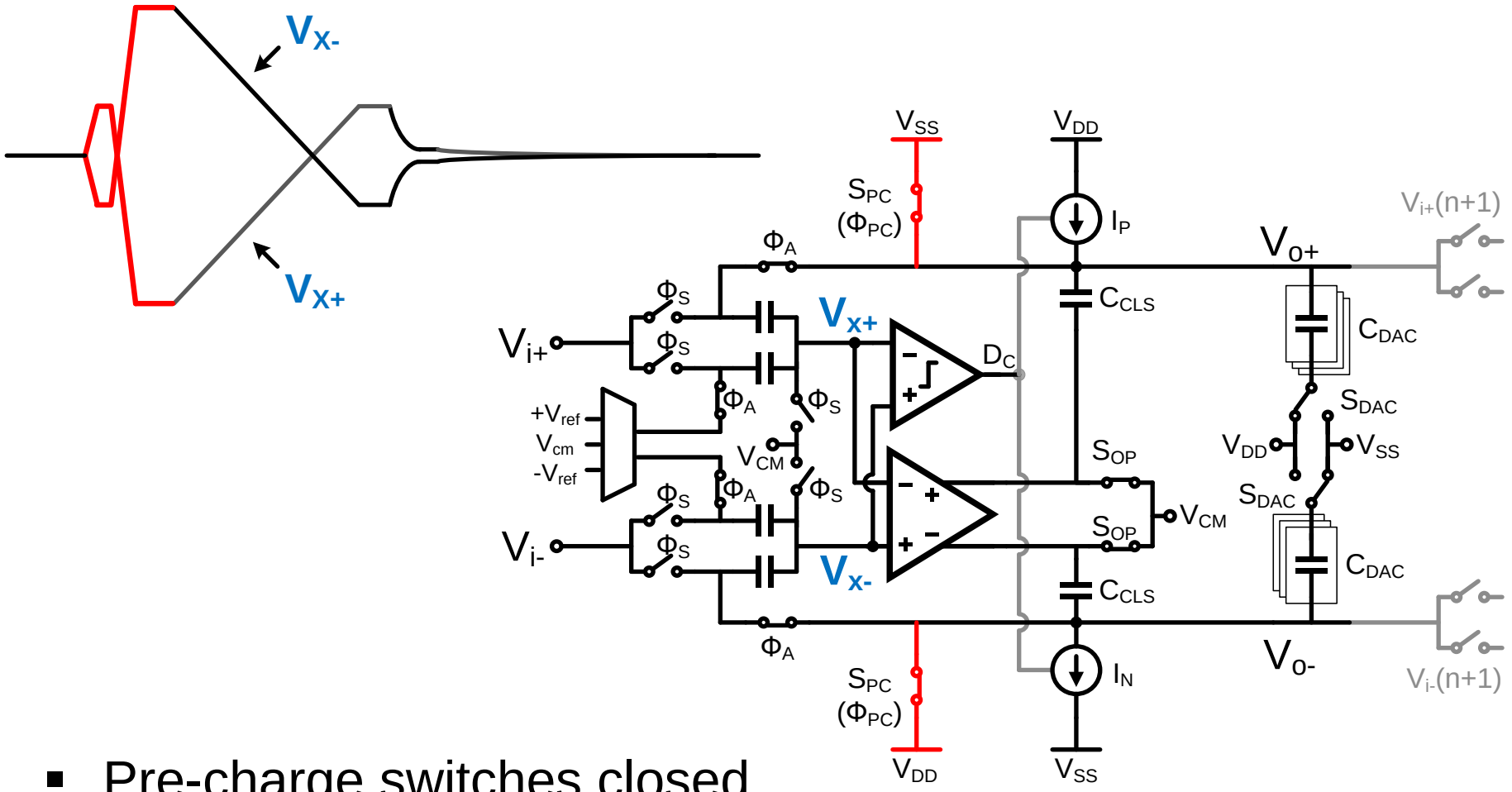


Hybrid CLS-Opamp/ZCBC

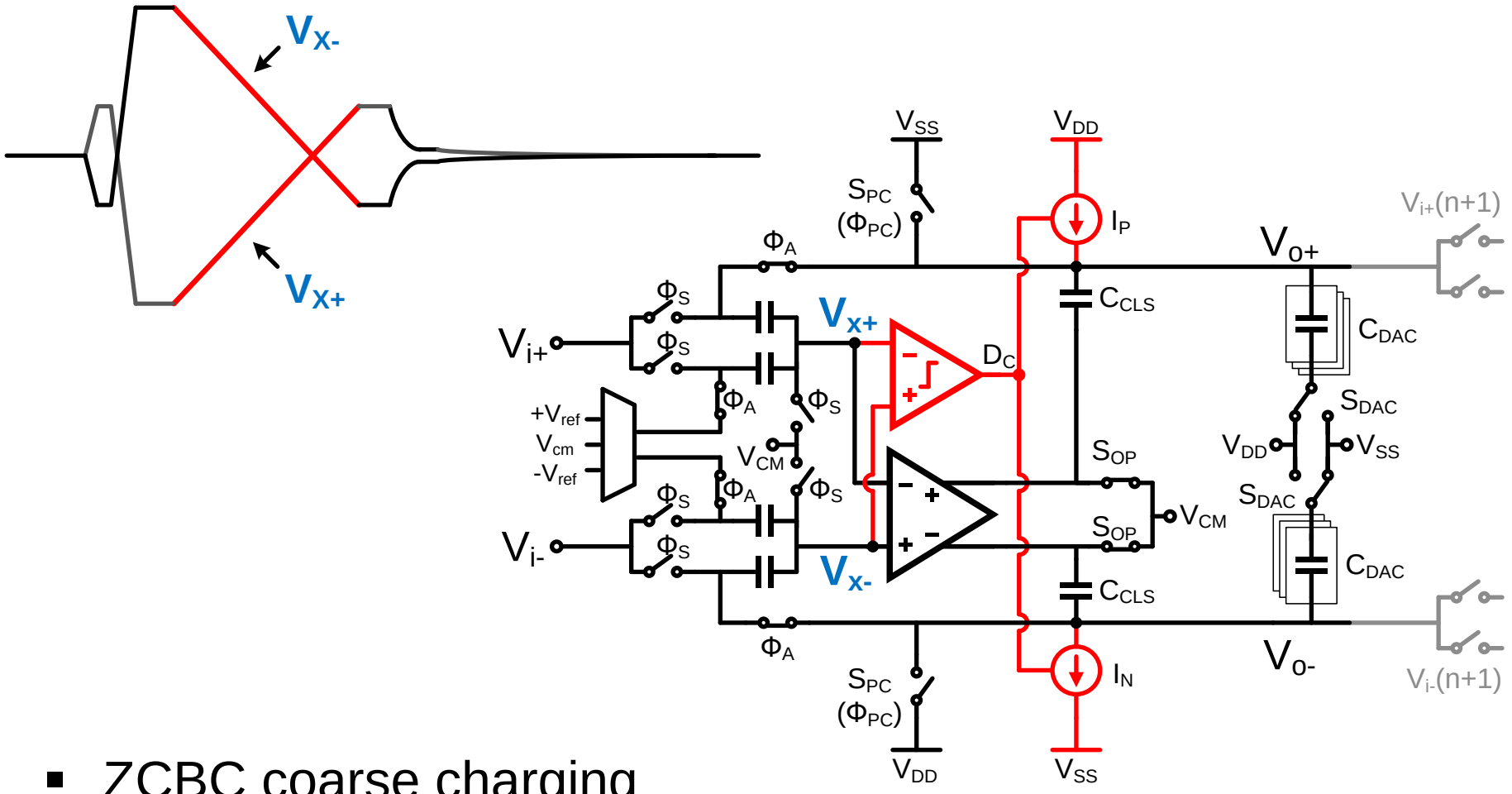


Hybrid CLS-Opamp/ZCBC

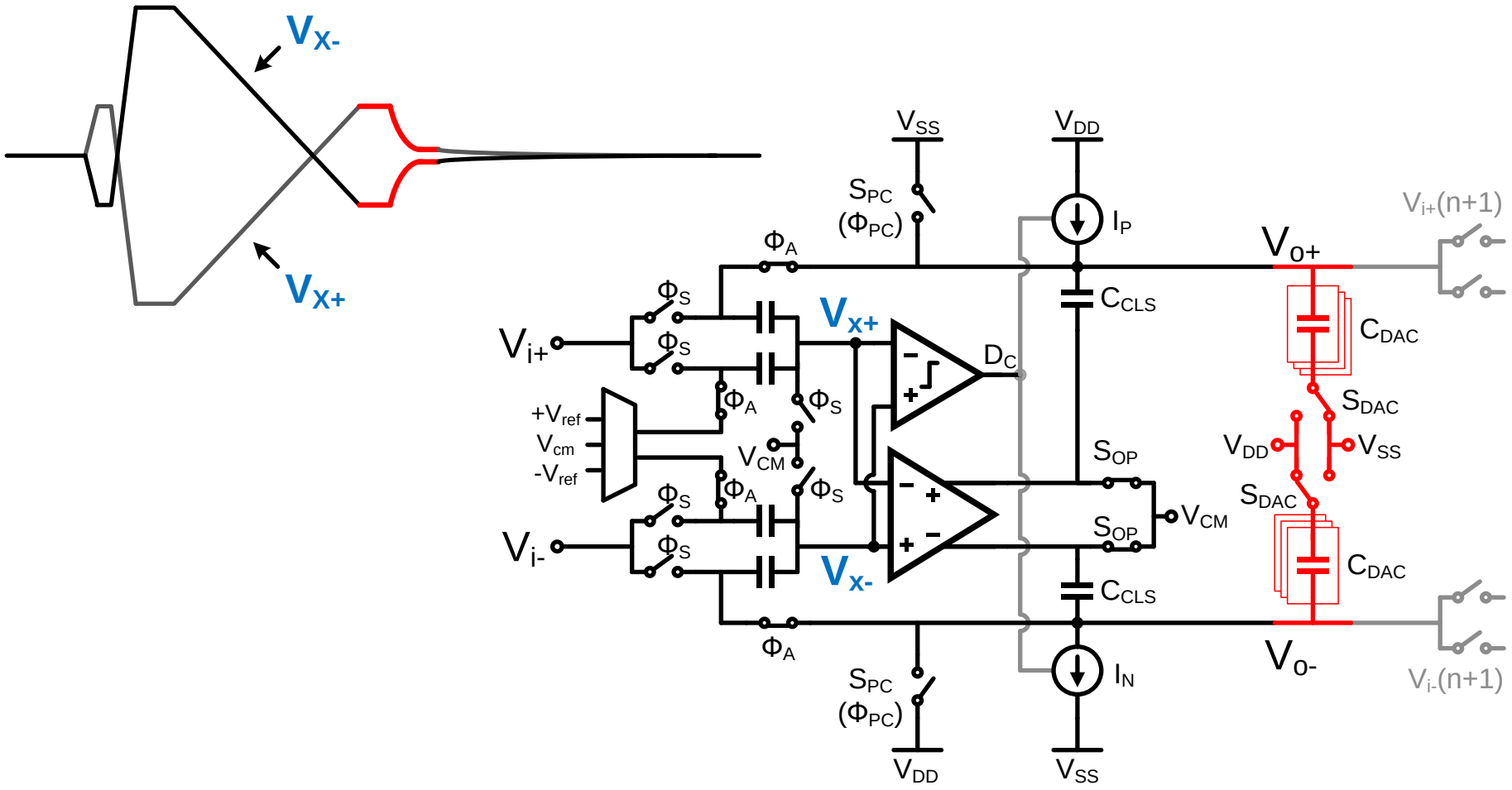




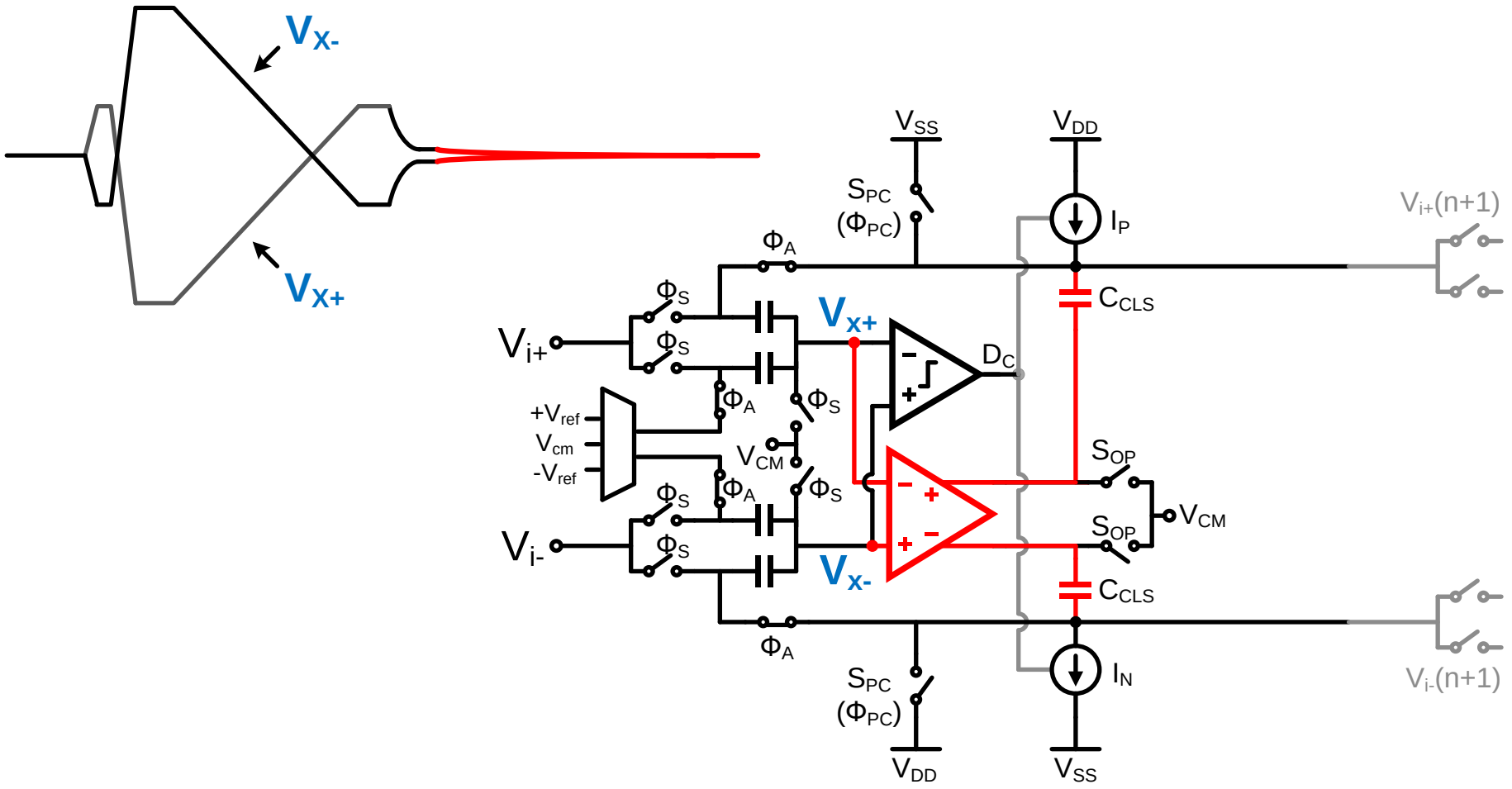
- Pre-charge switches closed
- ZCD & current sources begin to turn on
- Opamp output shorted to V_{CM}
- C_{DAC} set to track output



- ZCBC coarse charging
- When ZCD trips:
  - turns off current sources
  - activates asynchronous timing block

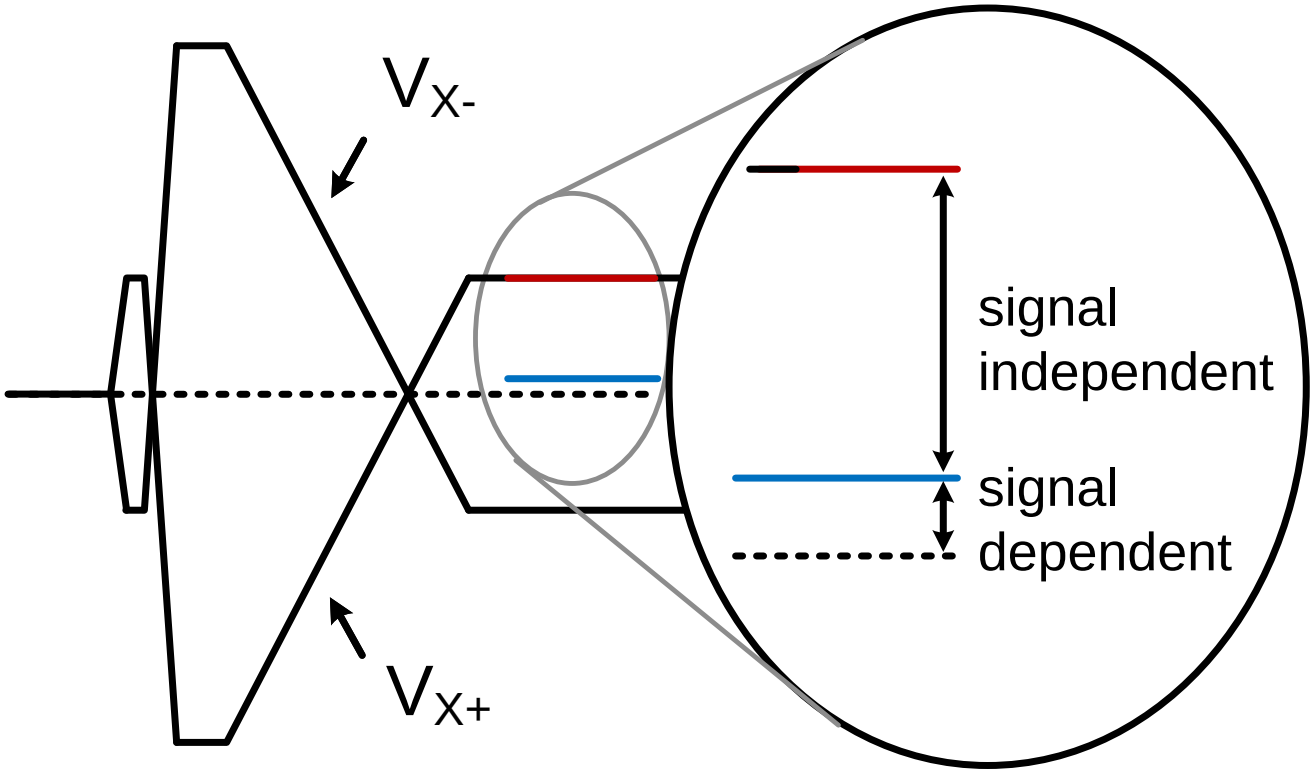


- Overshoot cancellation
- ΔV on bottom plate of C_{DAC} cancels overshoot



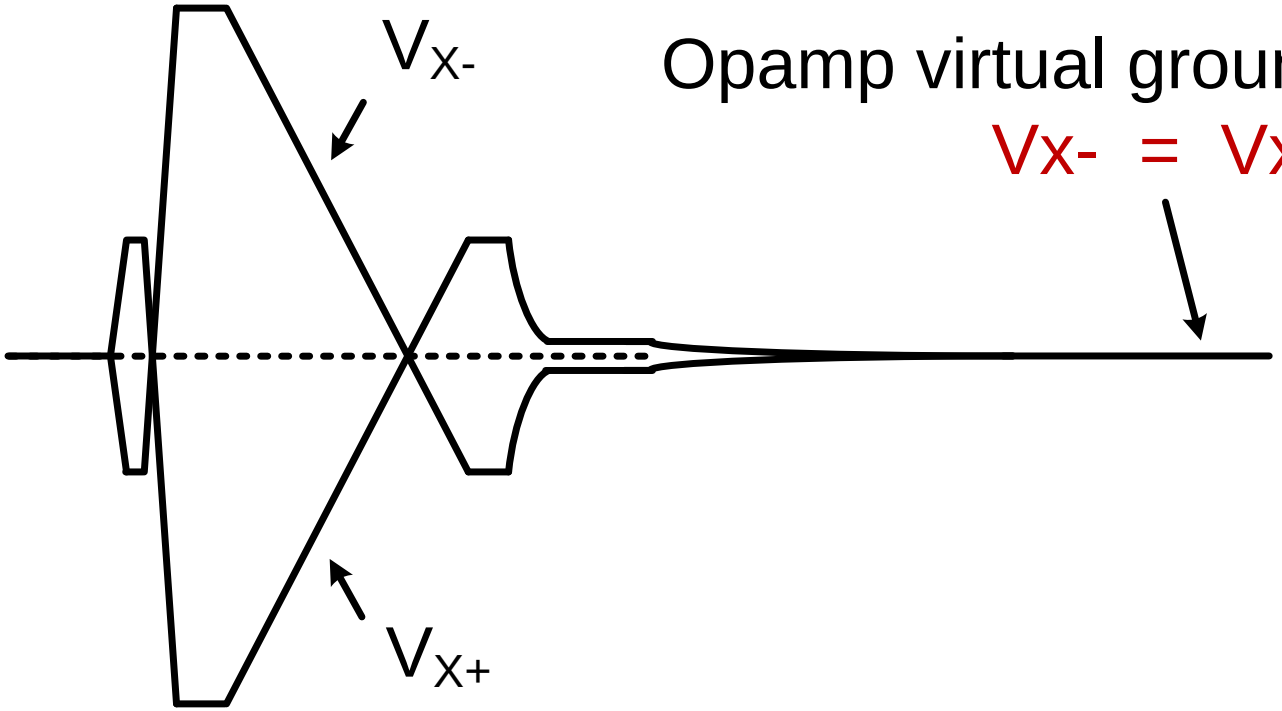
- Opamp fine settling
- Shorting switch (S_{OP}) opens
- C_{DAC} disconnects from output (minimize load)

Overshoot Cancellation



- Pure ZCBC: signal independent portion becomes DC offset
- Hybrid structure: opamp must cancel all overshoot

Overshoot Cancellation

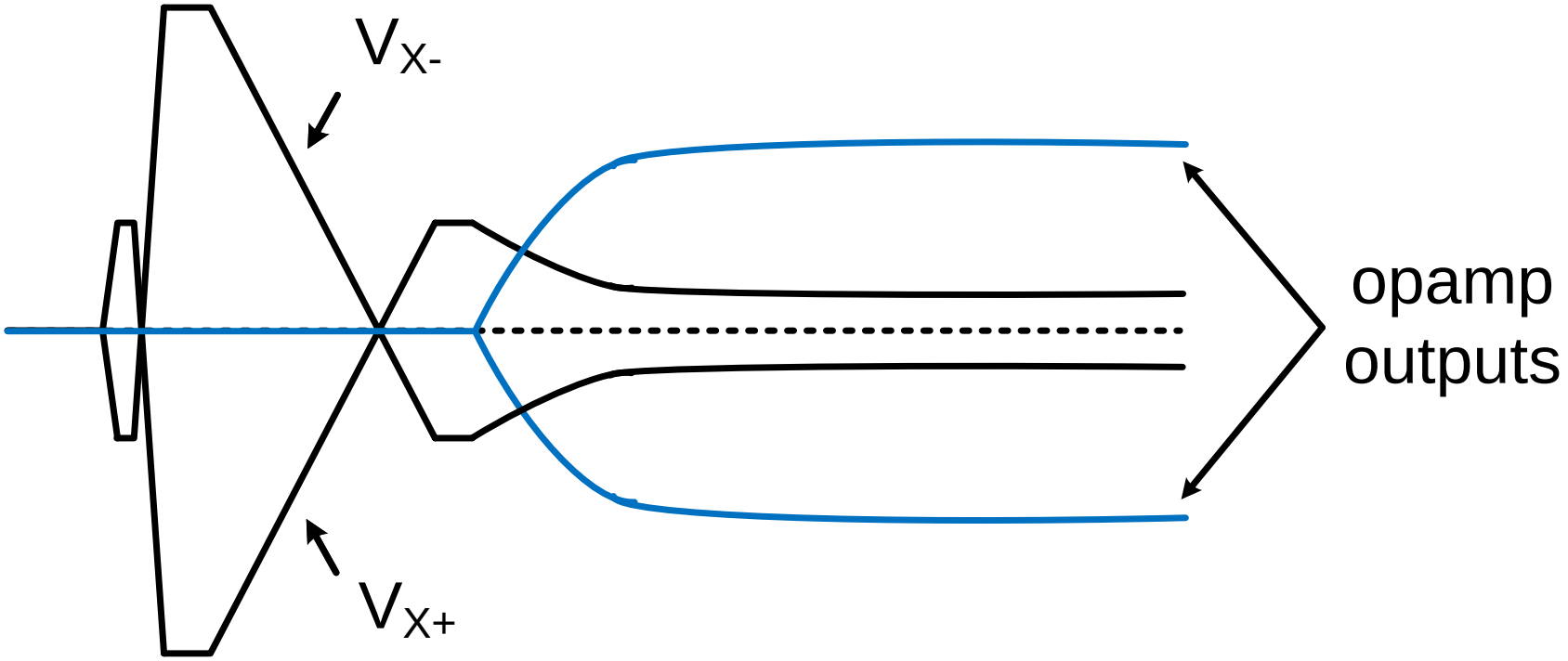


Opamp virtual ground condition:

Vx- = Vx+

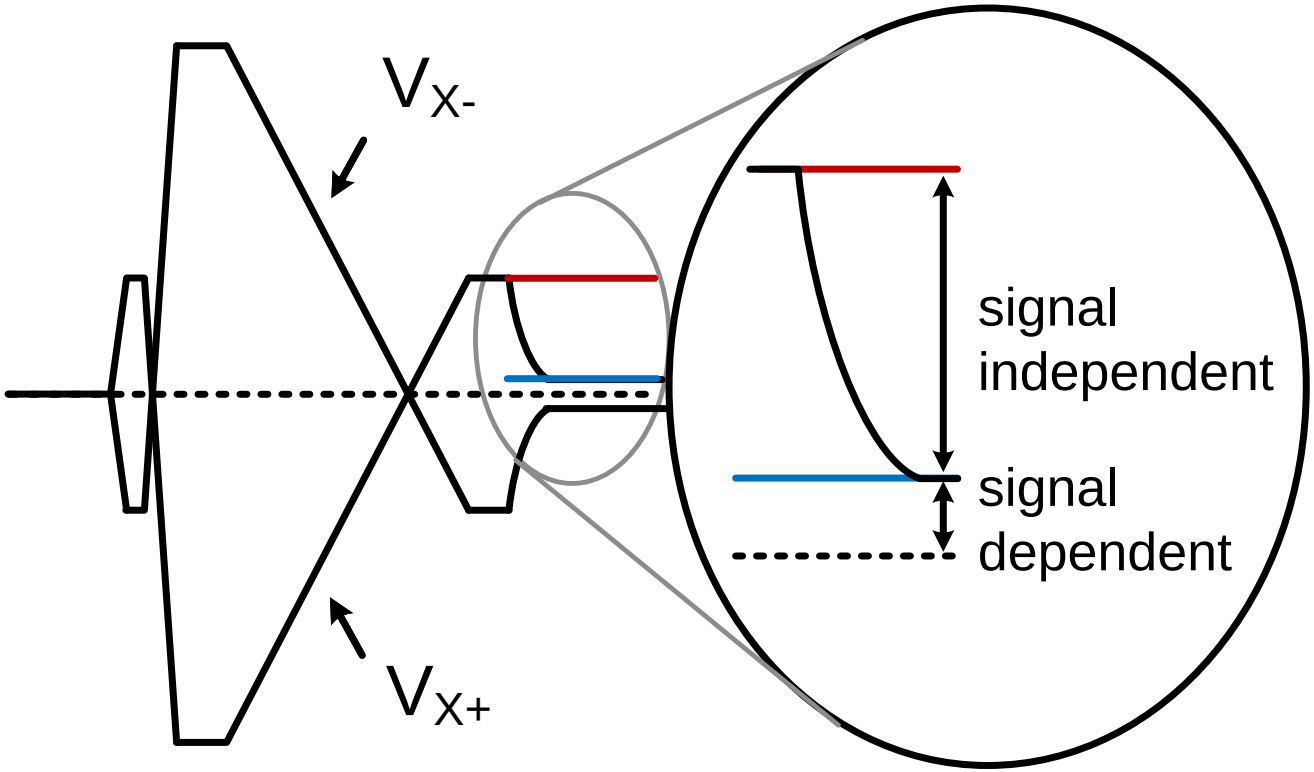
Opamp will try to cancel all overshoot present

Overshoot Cancellation



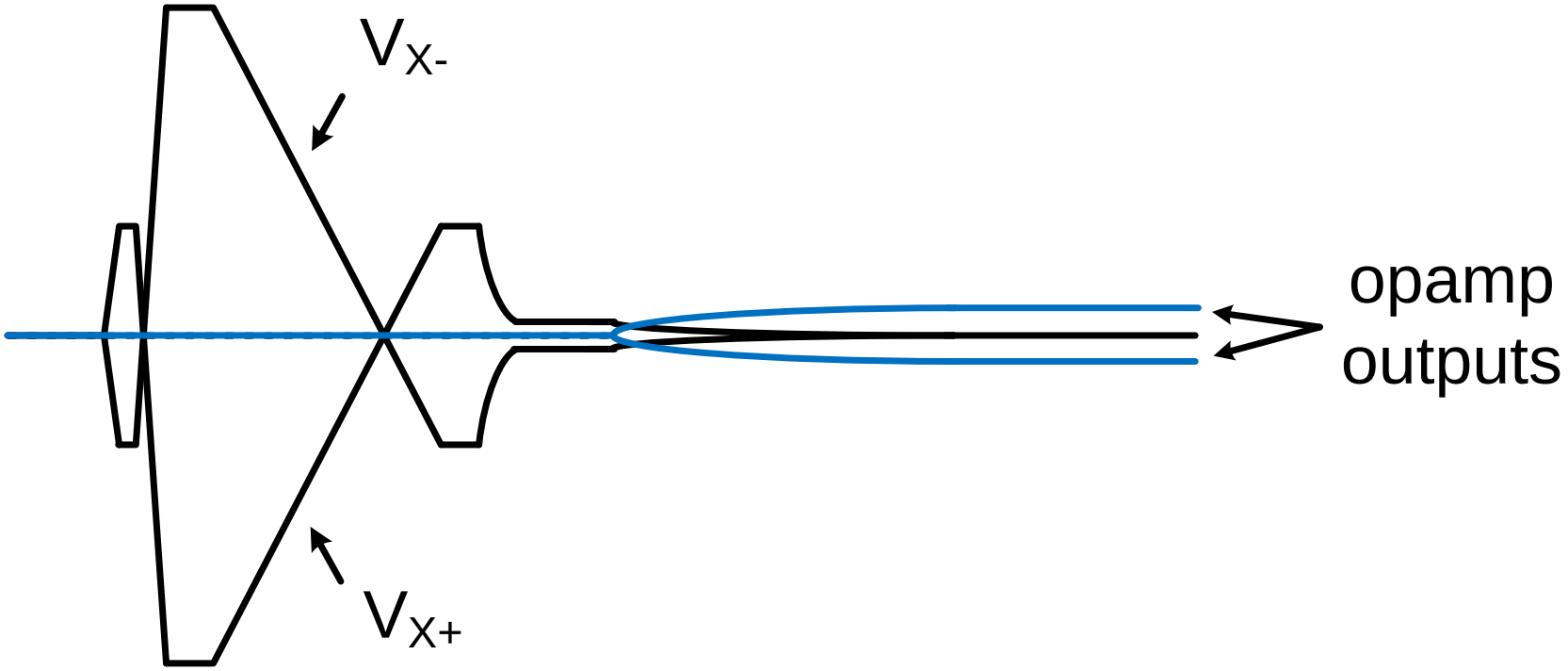
No cancellation: opamp output saturates

Overshoot Cancellation



A solution: cancel all predictable overshoot

Overshoot Cancellation

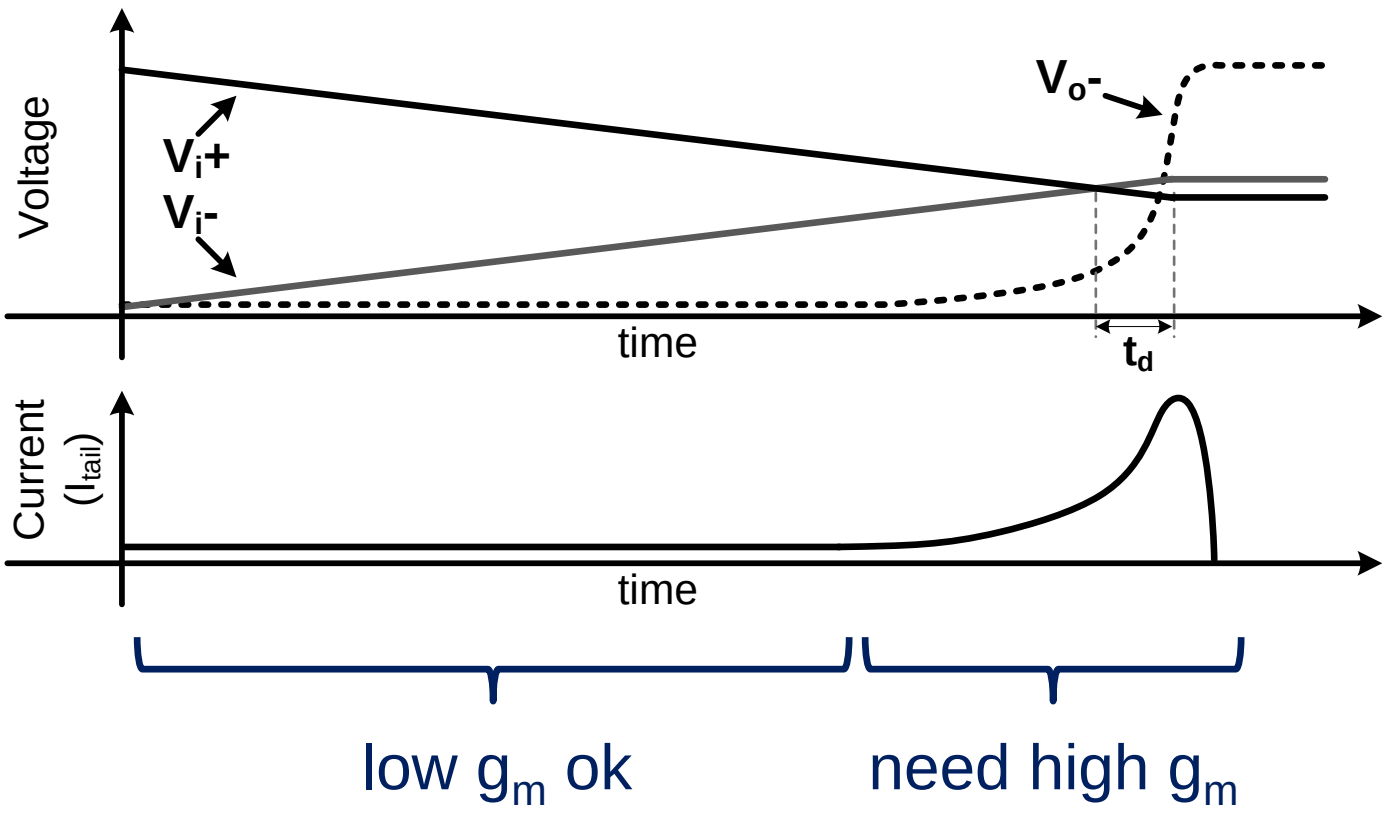


Opamp only processes signal dependent error

Overshoot Cancellation

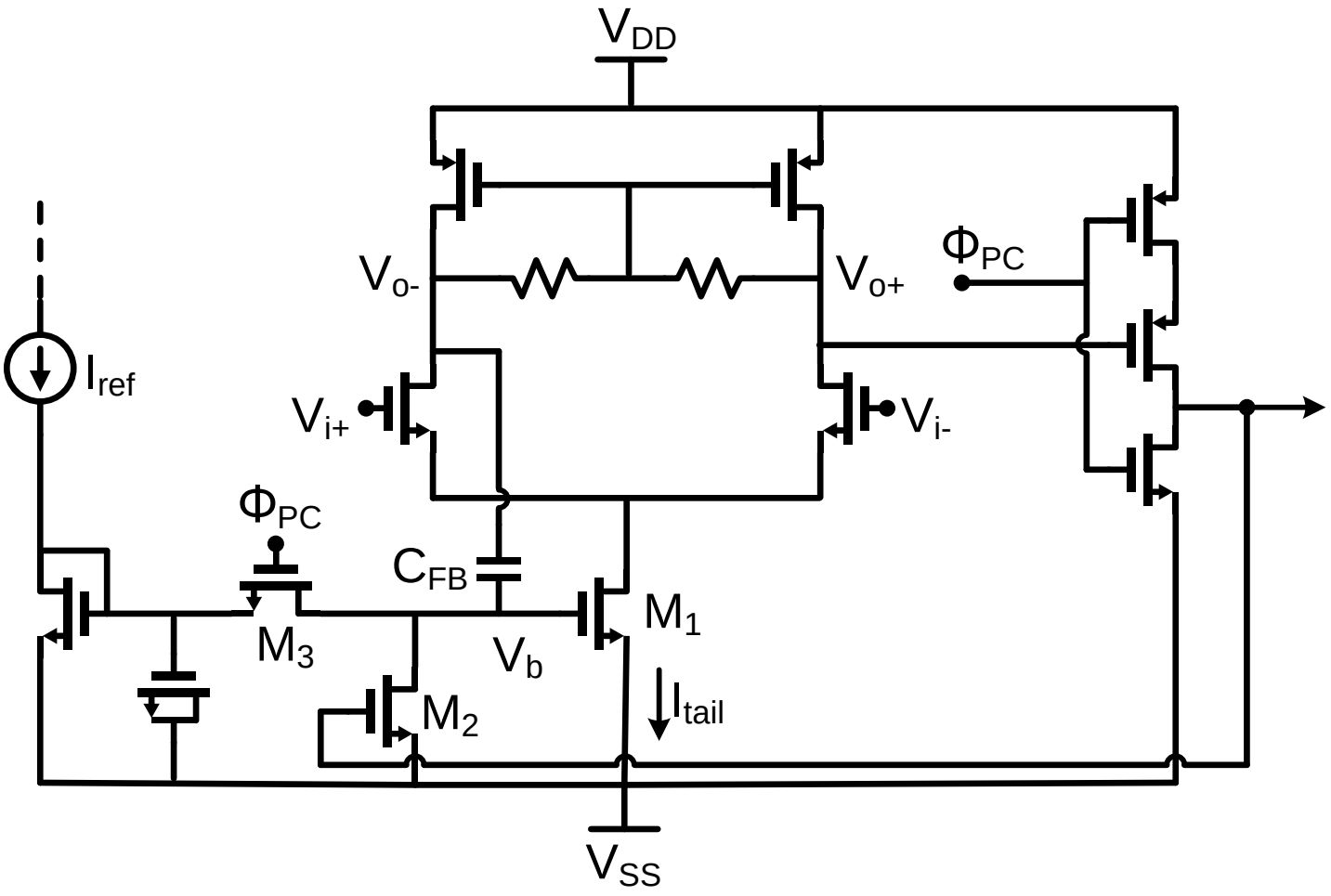
- Charge cancellation DAC
  - Testability
  - No offset accumulation
    - Integrator compatible (e.g. ΔΣ)
- Other possibilities to mitigate overshoot
  - ZCD input offset
  - Opamp input offset
  - Other DAC topologies

Dynamic ZCD

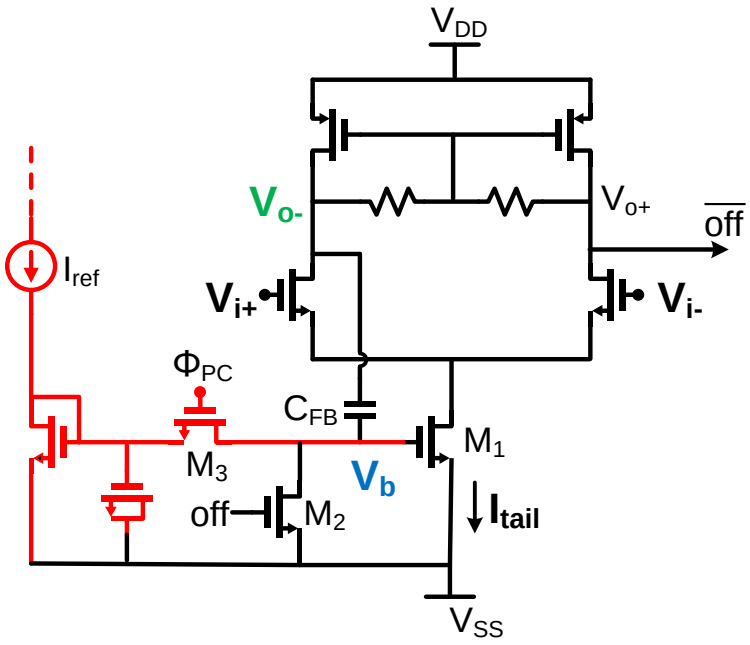


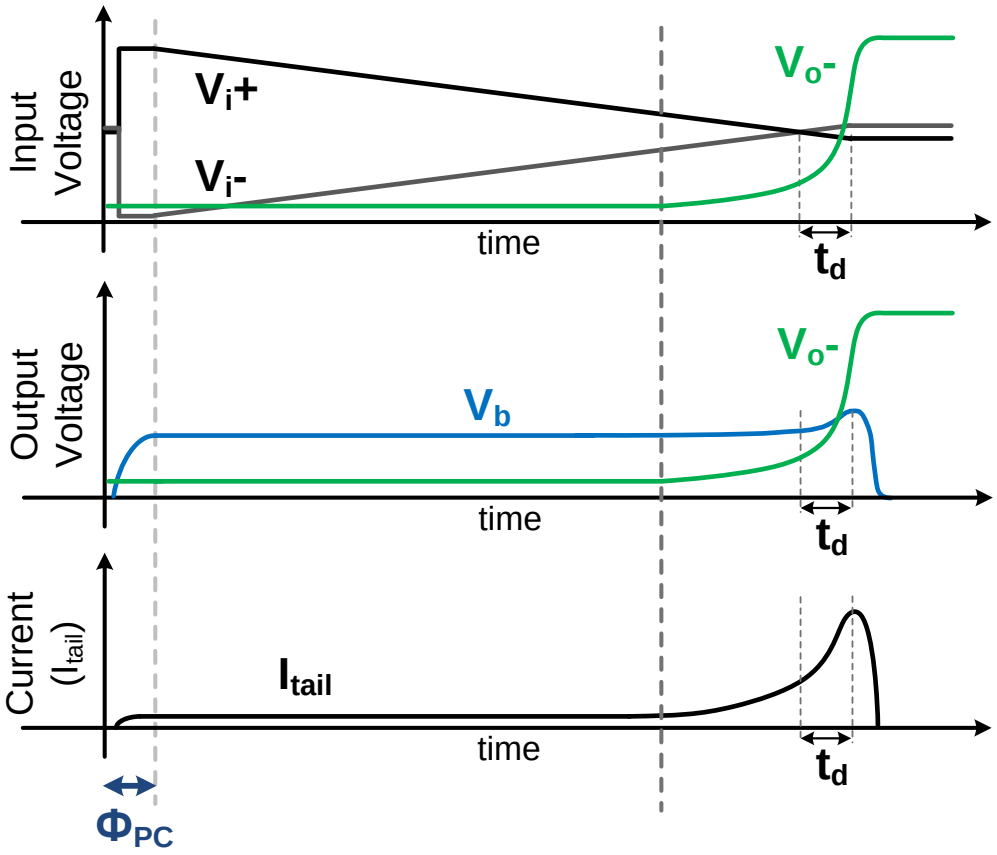
Concept: redistribute current usage to maximize useful g_m

Dynamic ZCD



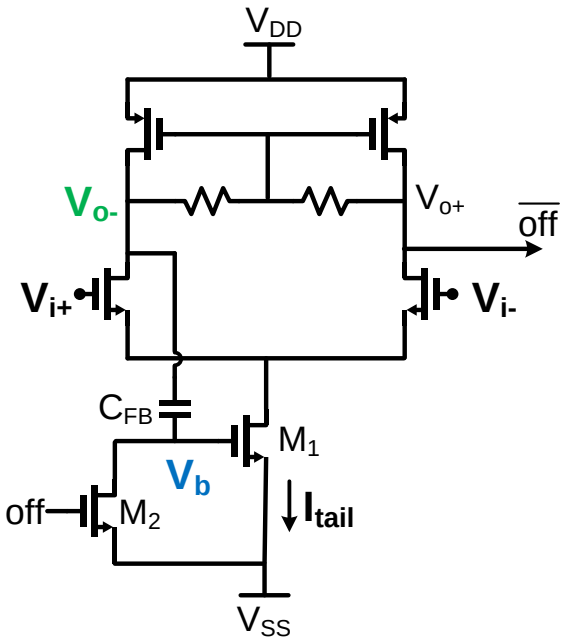
Dynamic ZCD

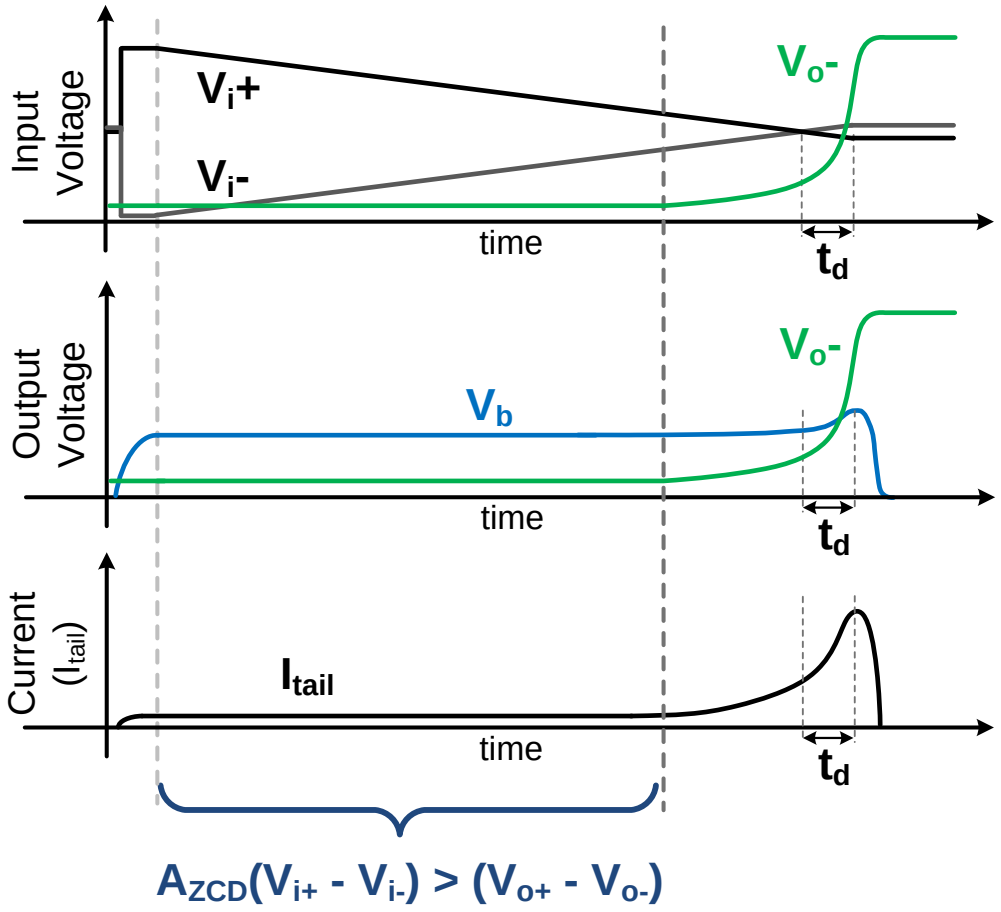




Step 1: Pre-charge

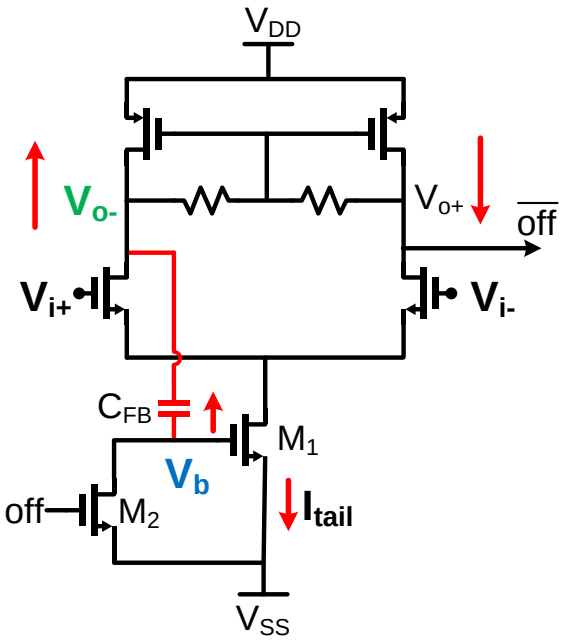
Dynamic ZCD

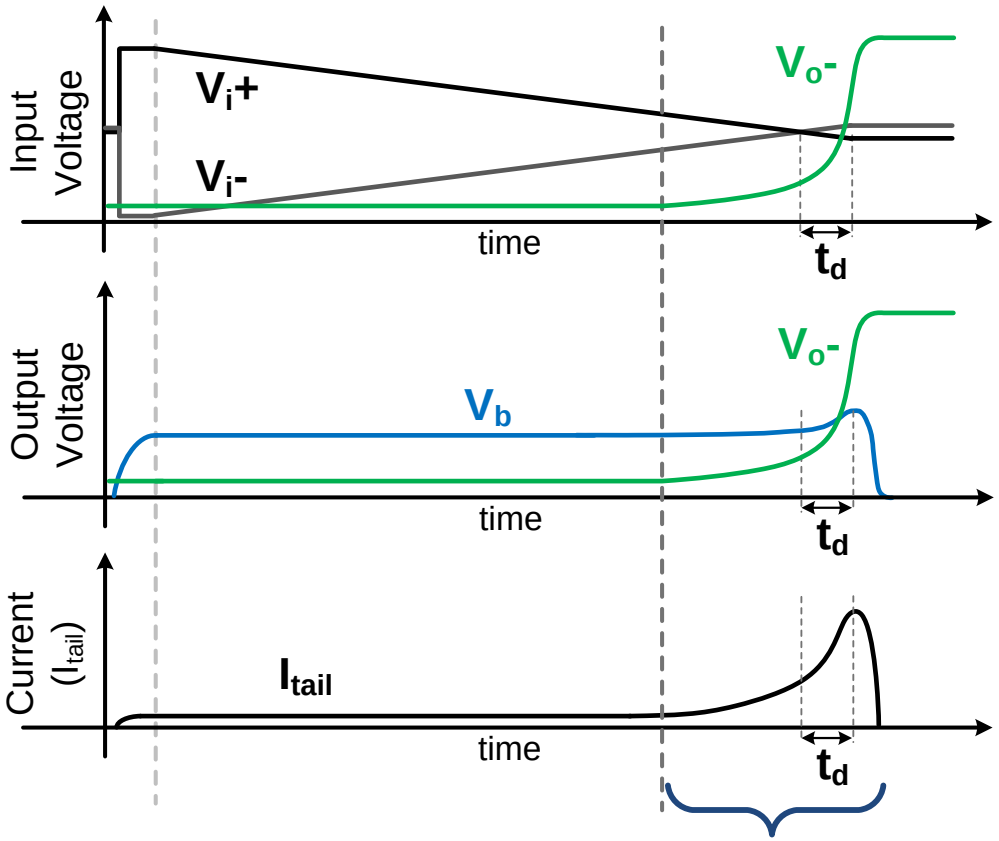




Step 2: Power conservation

Dynamic ZCD

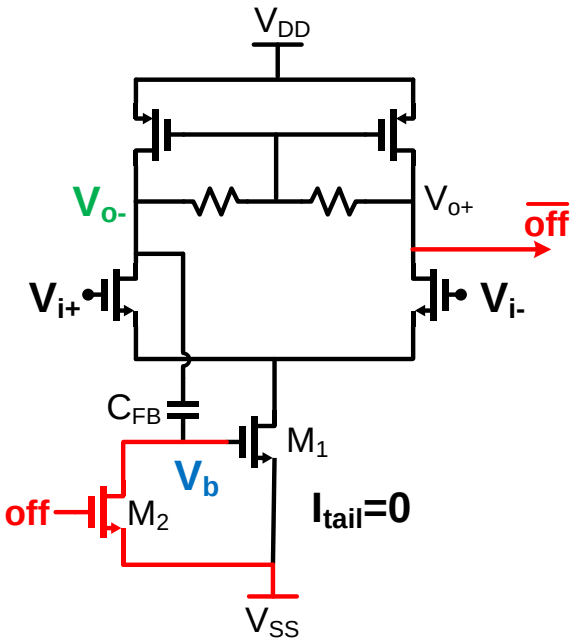


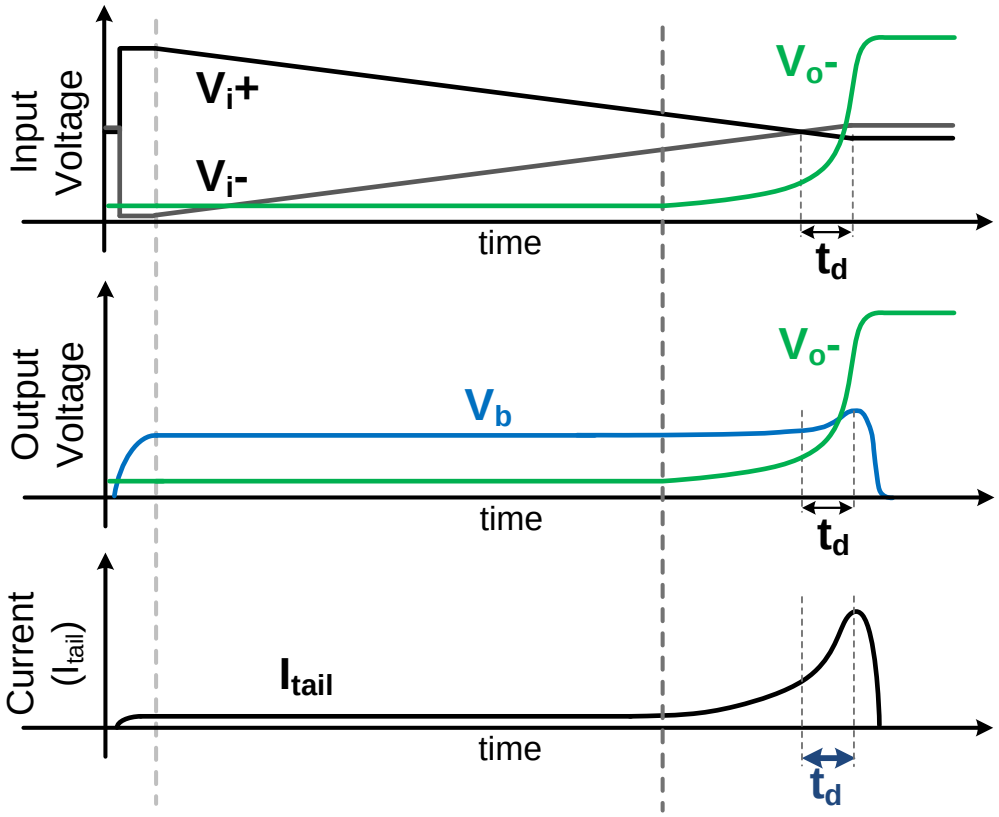


$A_{ZCD}(V_{i+} - V_{i-}) < (V_{o+} - V_{o-})$

Step 3: High g_m

Dynamic ZCD





Step 4: Shutdown

Dynamic ZCD

- Strongly correlated design variables
  - A_{ZCD}
  - C_{FB}
  - I_{SRC}/C_{LOAD}
- Best choice dependent on specific design targets

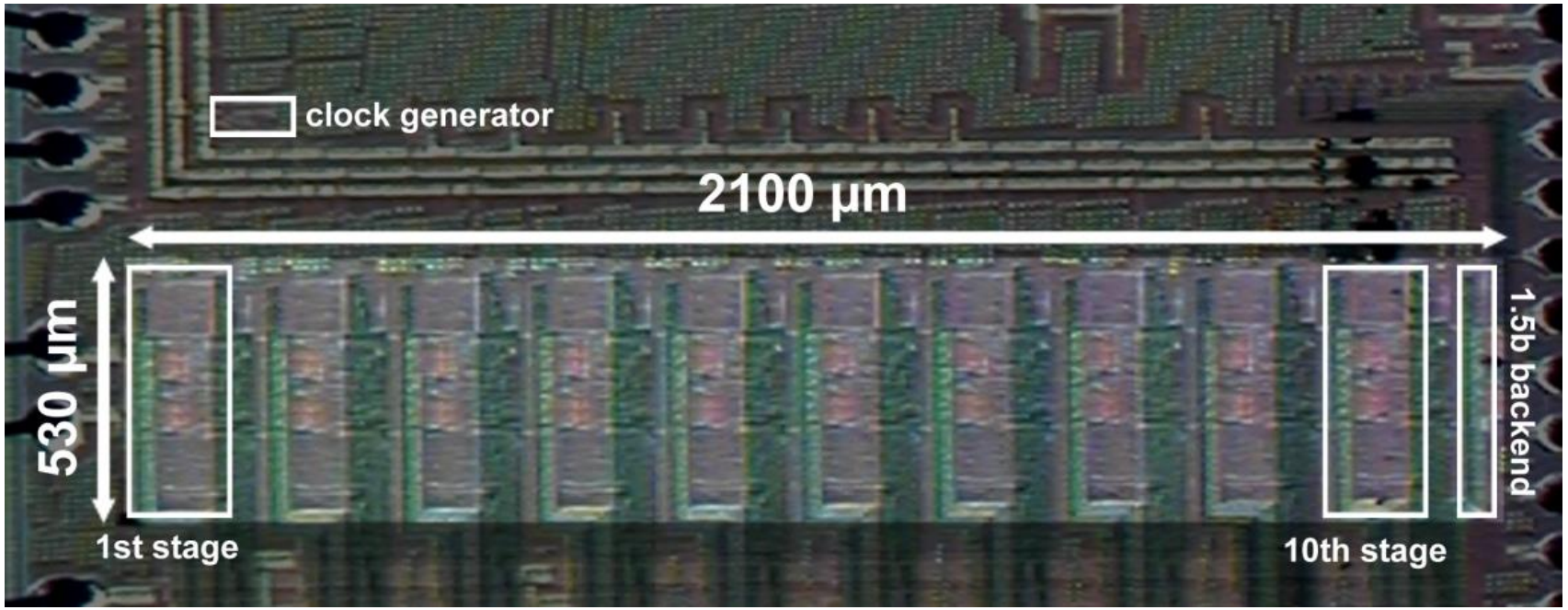
ZCD Variation Tolerance

- In test, I_{ref} varied from 6.5uA - 50uA with no impact on performance
  - Only limited by tuning range of test board
  - Current bias, voltage bias, or self-bias feasible
- Higher g_m at critical instant can suppress certain internal and external variations
- Floating bias
  - Blocks certain transient effects
  - Vulnerable to others

ZCD Power Efficiency

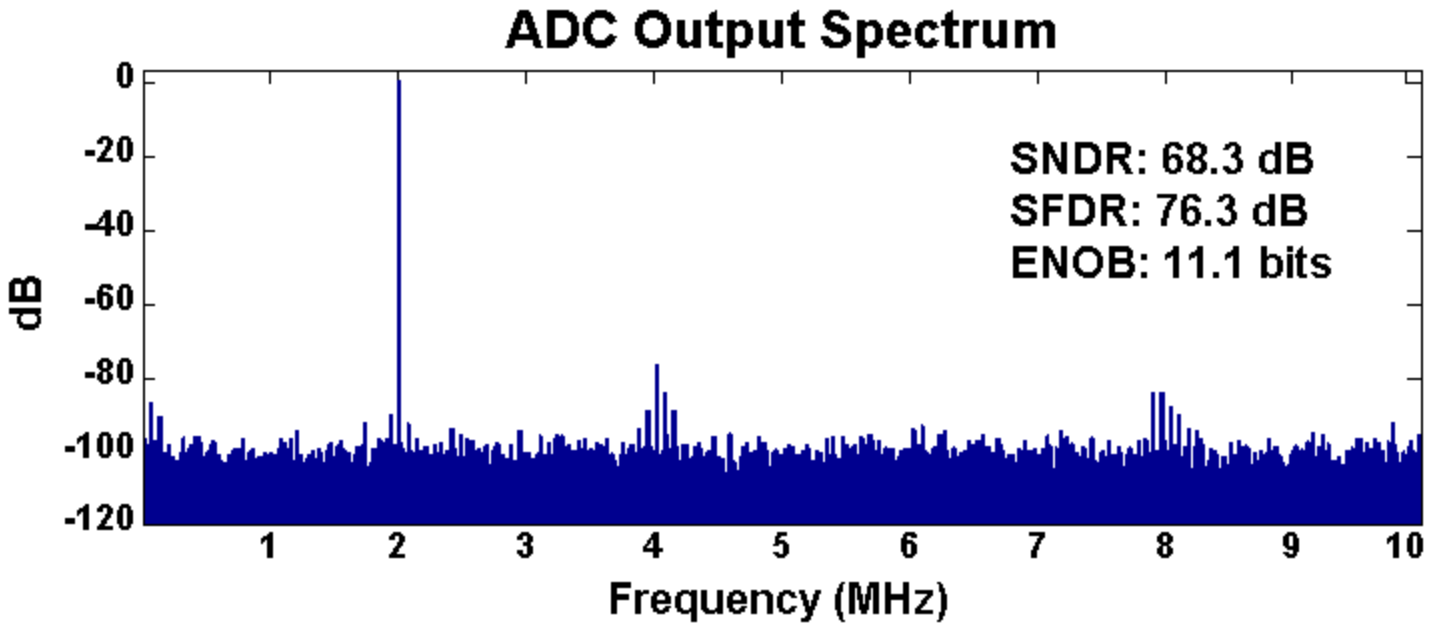
- Your mileage will vary
- Depends on design specifications
  - Converter accuracy
  - ZCD time delay
  - Current source slew rate
- For this test ADC: simulation shows 4x improvement over state of the art (*Brooks, ISSCC 2009*)
- In general, the slower the ramp, the more dramatic the savings

Chip Micrograph

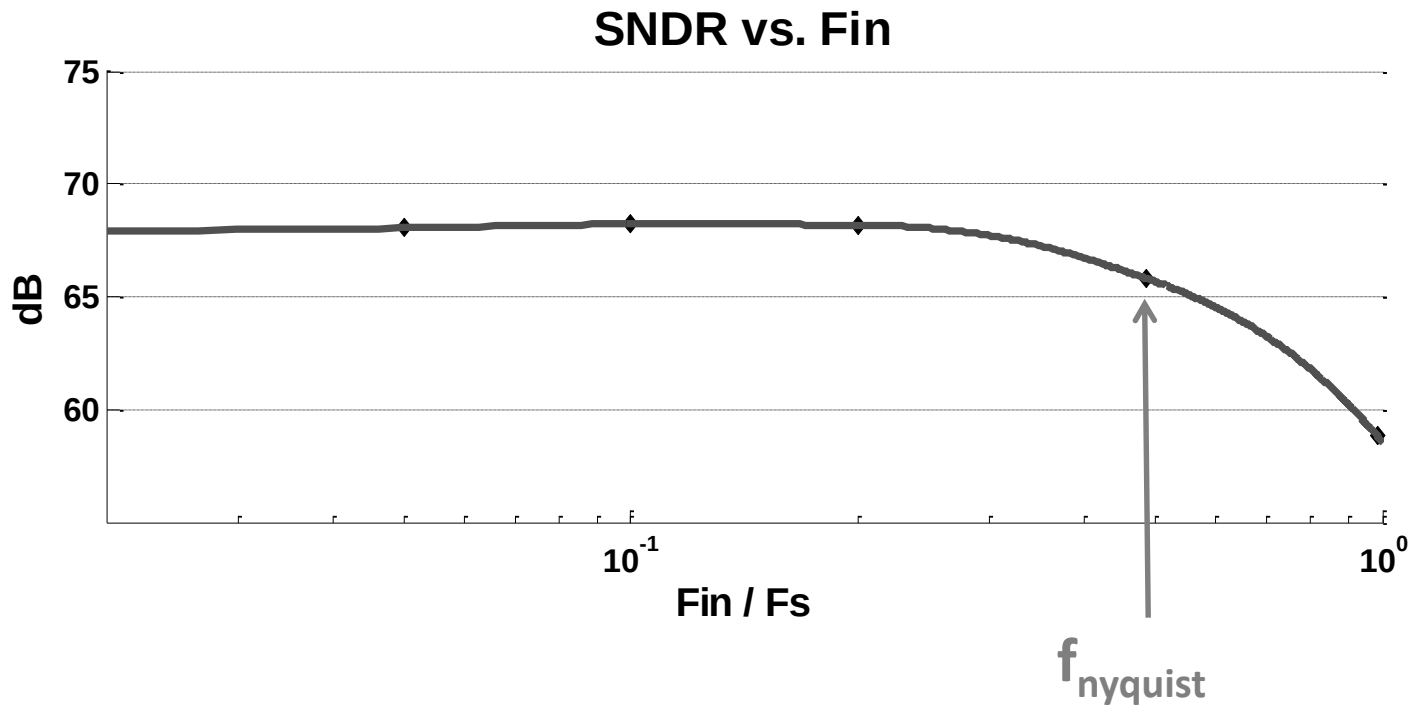


- 10 identical 1.5b stages
- 1.5b backend flash

Measured Results



Measured Results



Measured Results

Technology	0.18μm CMOS			
Supply Voltage	1.8V			
Input Voltage Range	1.4V			
Sampling Frequency	f_S = 10 MHz		f_S = 20 MHz	
ENOB	11.3b		11.1b	
SNR	69.6dB		68.3dB	
SNDR	69.5dB		68.3dB	
SFDR	78.8dB		76.3dB	
Power (analog/digital)	7.2mW	1.2mW	15.0mW	2.2mW
FoM	343.5 fJ/step		405.5 fJ/step	

Key Benefits

- Accuracy - Extremely high effective gain, even in modern processes.
- Robustness - Relax ZCBC design by adding linear feedback.
- Efficiency - Amplification devices optimized for unique requirements. Efficient charging with ZCBC. High gain, single stage opamp w/o gain boosting amplifiers or compensation.

Acknowledgements

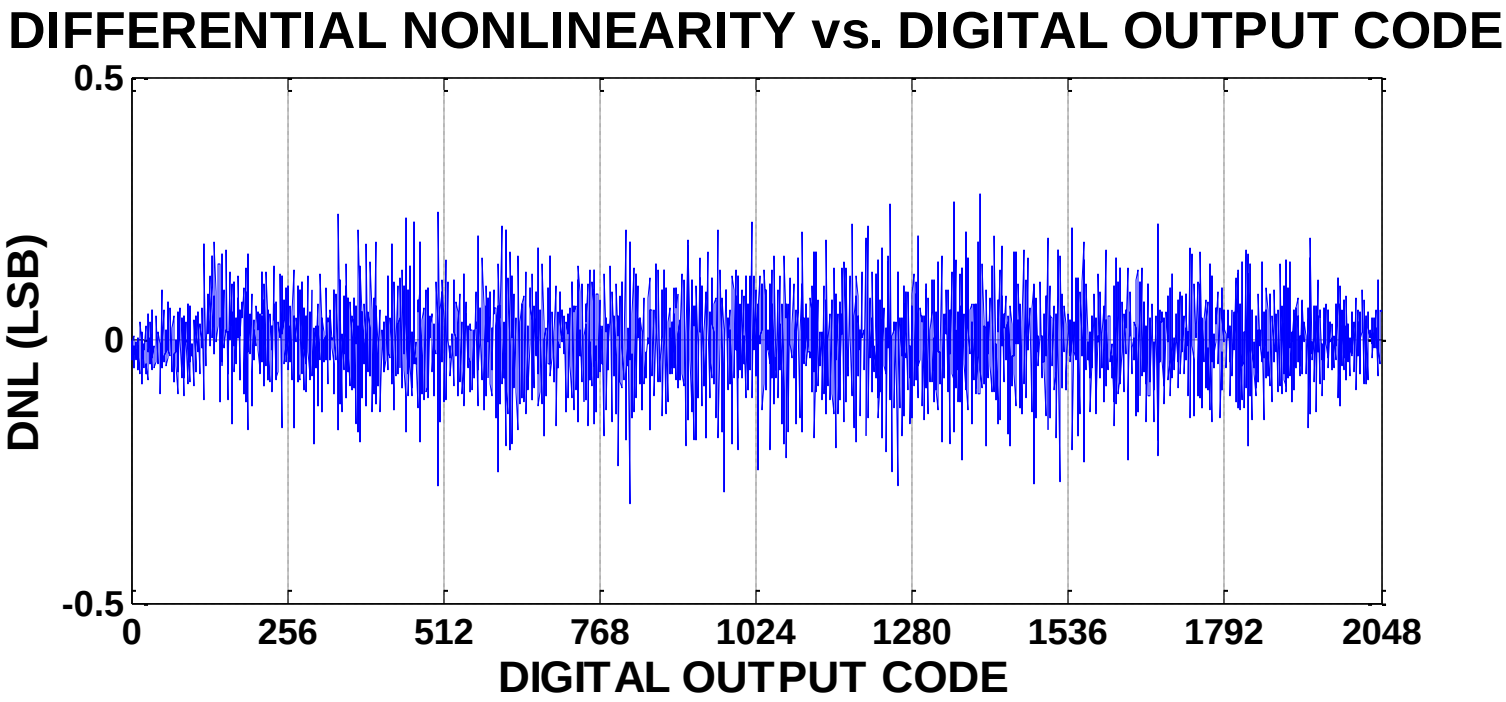
- This work was funded by the Semiconductor Research Corporation and the Center for Design of Analog-Digital Integrated Circuits.

- The authors would like to thank TowerJazz Semiconductor for providing fabrication.

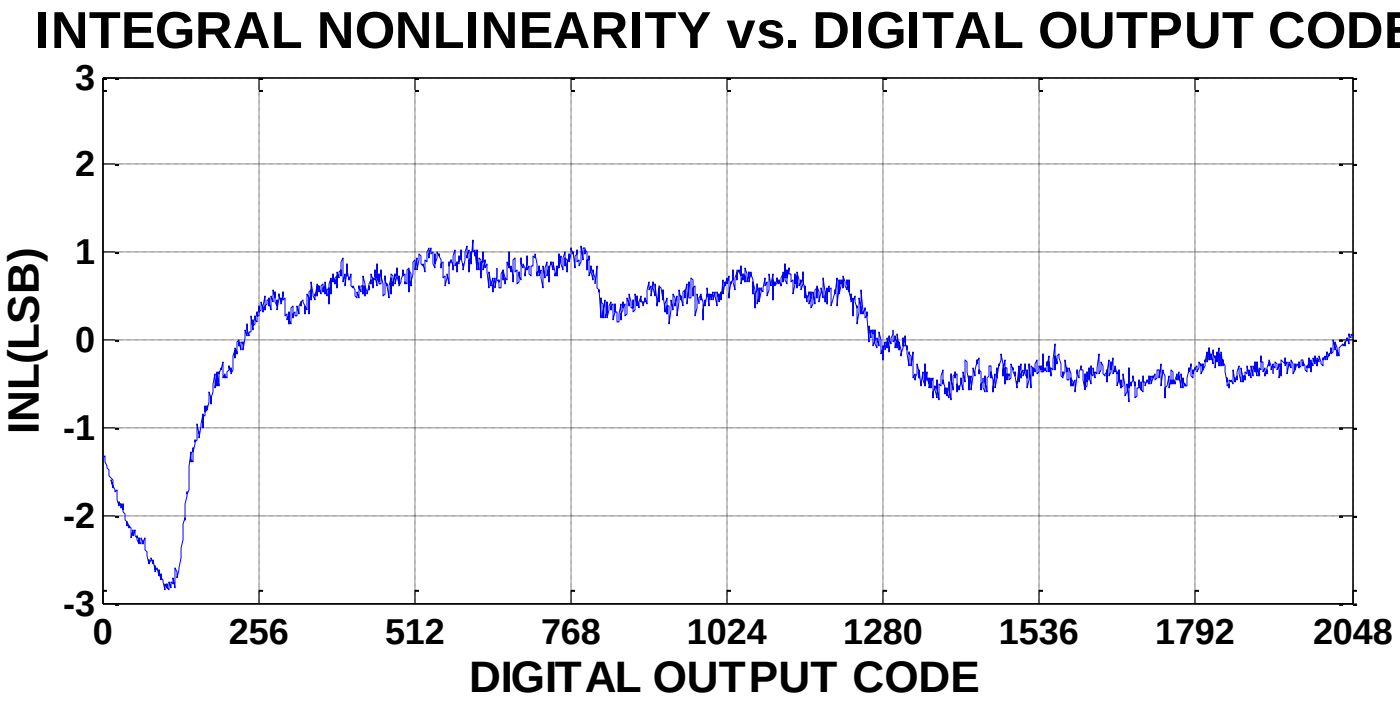
Additional thanks to Peter Kurahashi, Sasidhar Lingam, Phil Crosby, Arnie Frisch, Ed Hershberg, Dianne Glenn and members of the OSU AMS lab for their valuable contributions and insight.

Additional Materials

DNL

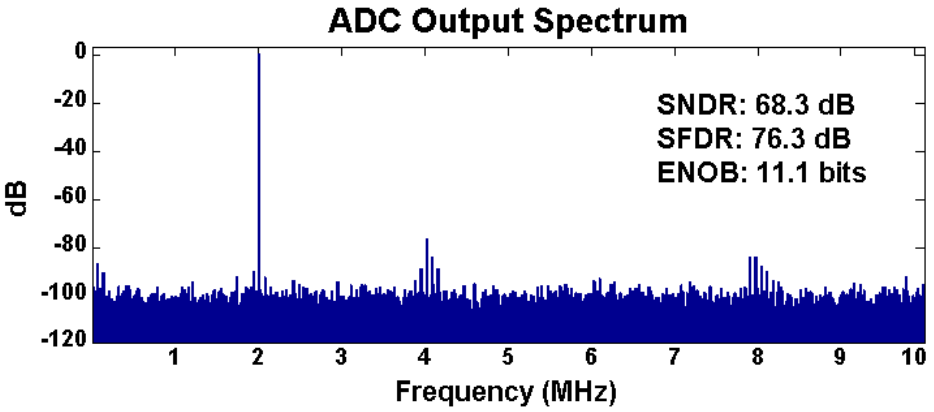

DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE
DNL (LSB)
0.5
0
-0.5
0
256
512
768
1024
1280
1536
1792
2048
DIGITAL OUTPUT CODE

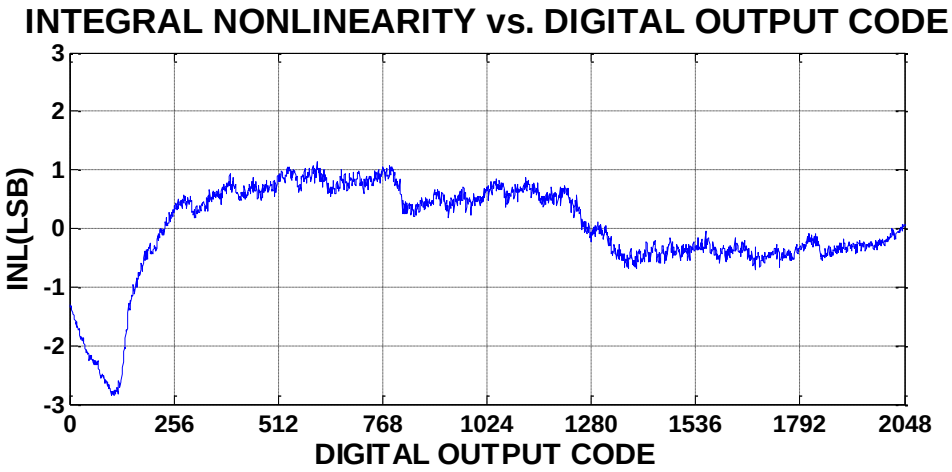
INL


INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE
INL(LSB)
3
2
1
0
-1
-2
-3
0
256
512
768
1024
1280
1536
1792
2048
DIGITAL OUTPUT CODE

Hypothesis for distortion issue

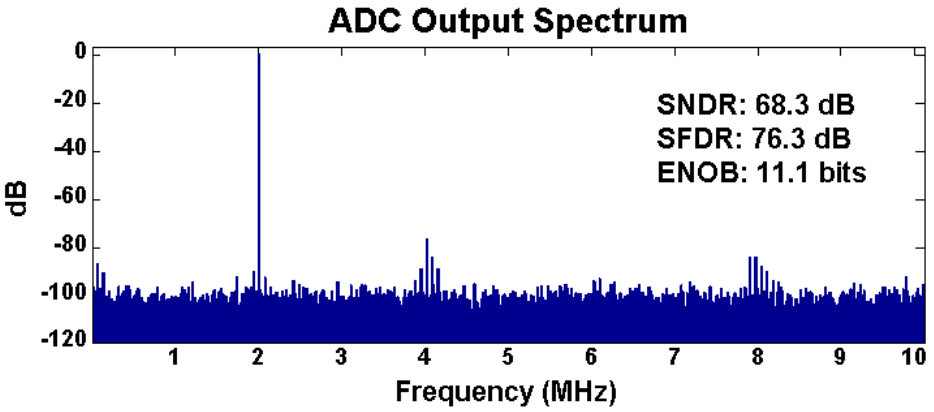
- Even harmonics not seen in previous version of test board
- Possibly originates from off-chip
- However, there is also an on-chip explanation…

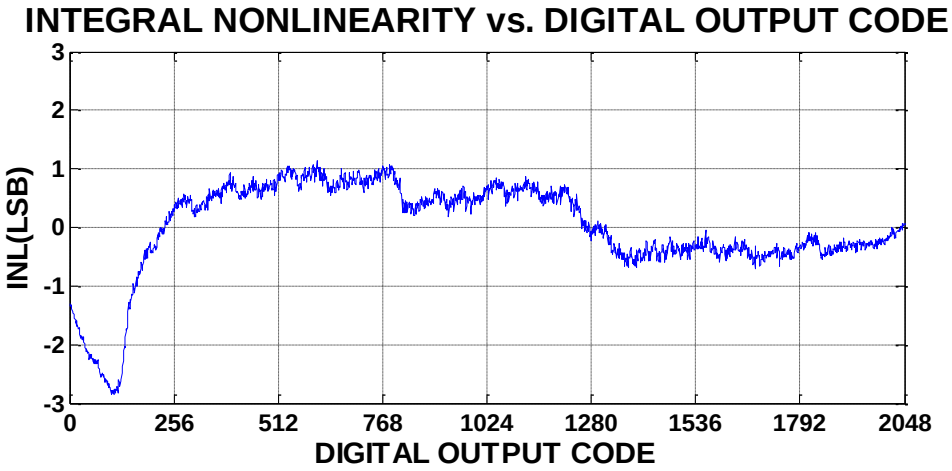




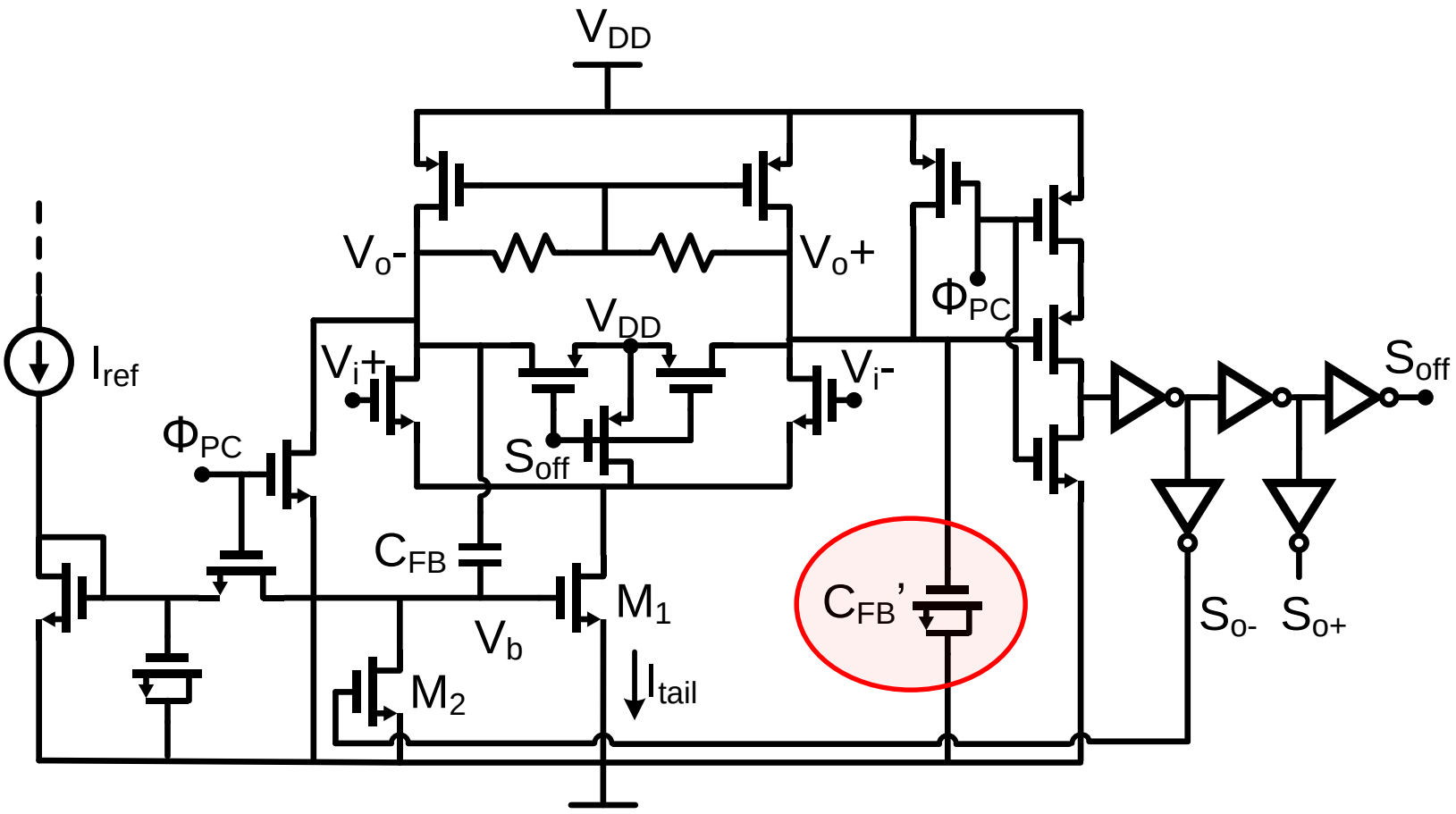
Hypothesis for distortion issue

- If inputs begin too close together (i.e. lowest codes), there will be a large variation in ZCD time delay
- Need to be careful that asymmetry of dynamic ZCD doesn't cause an input offset that will worsen this performance "wall"





Hypothesis for distortion issue

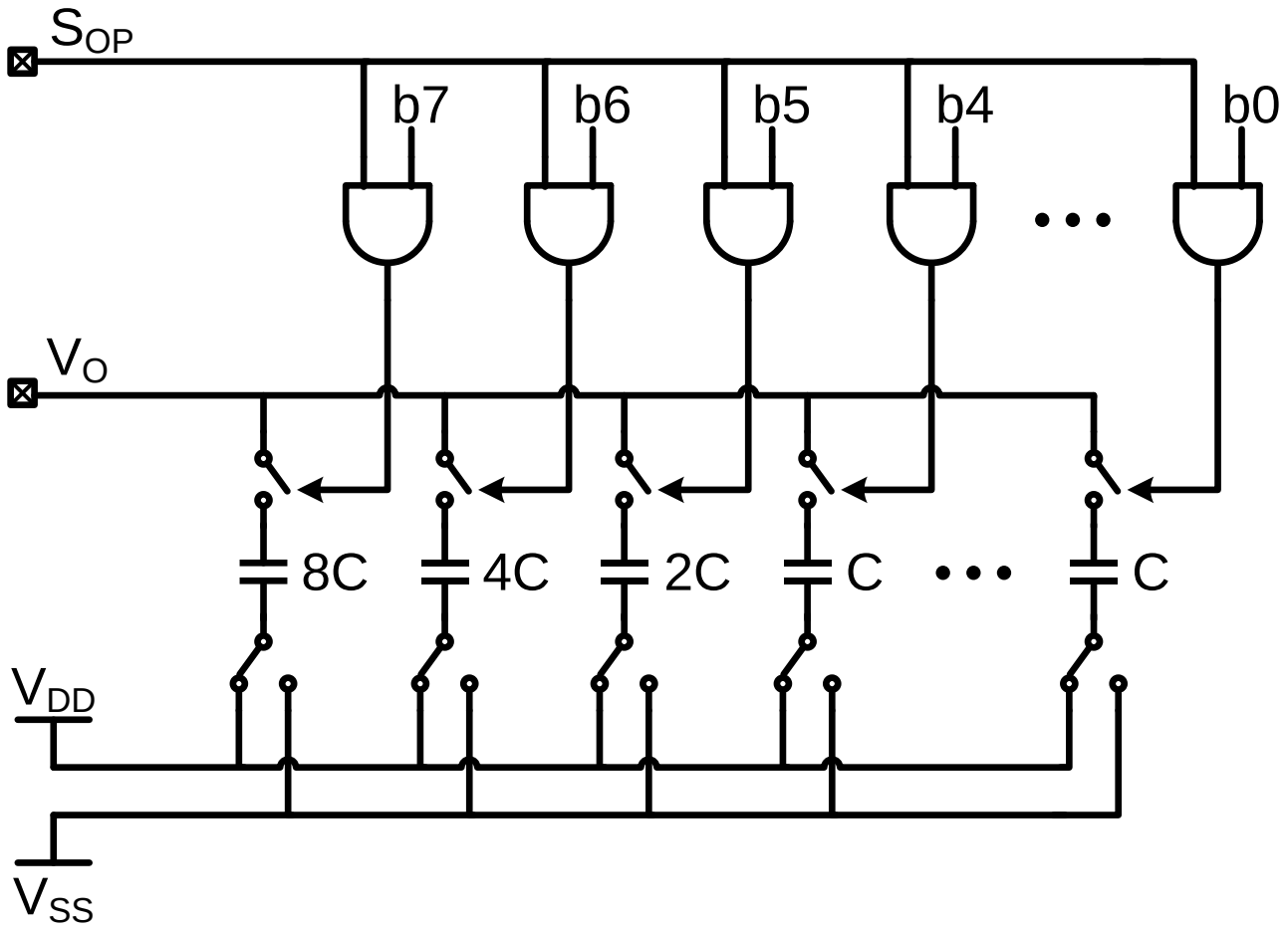


Needed more analysis to determine the best value for the dummy load

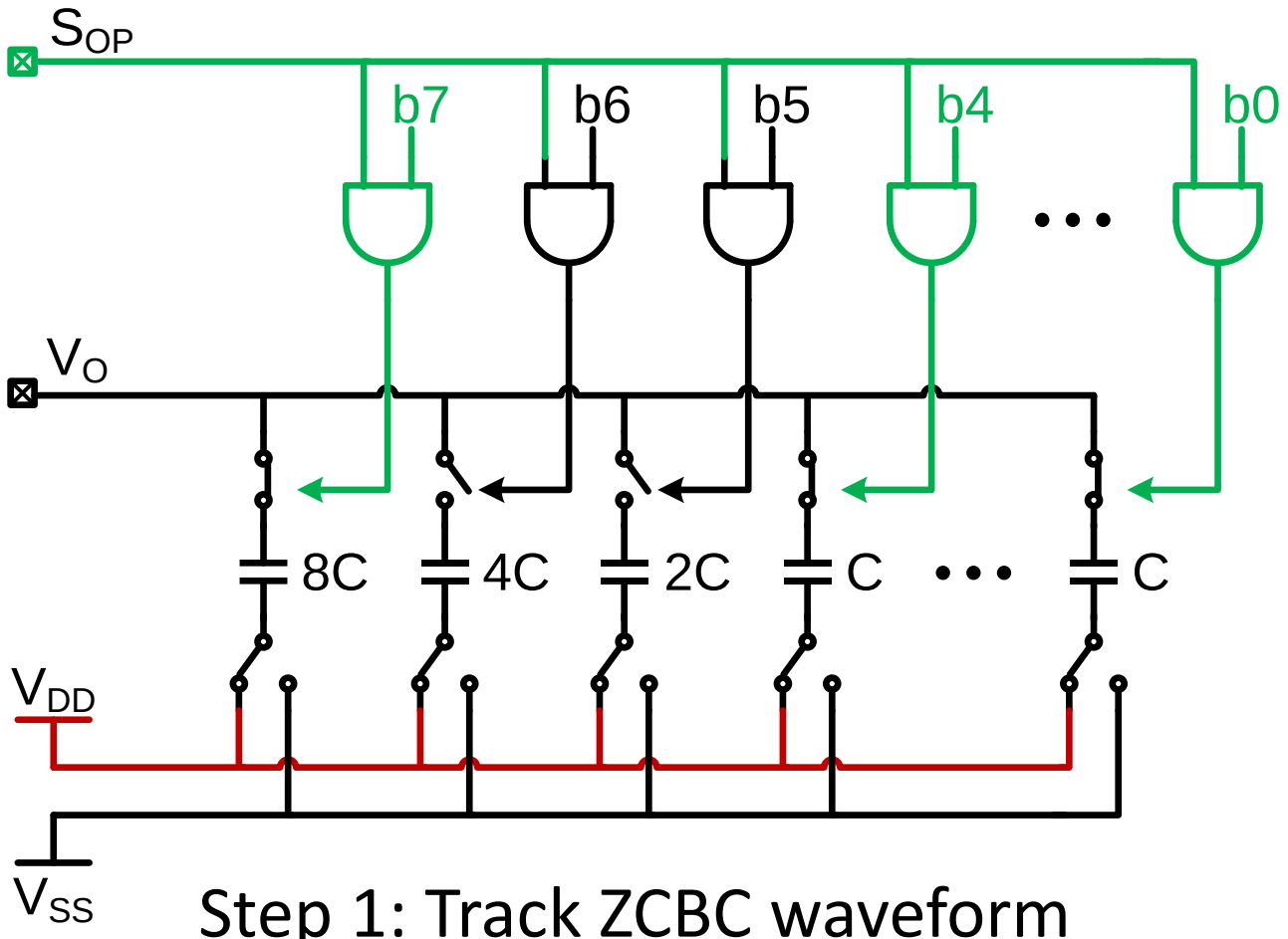
Overshoot Cancellation

- Independent digital controls for each stage
  - Vo+ and Vo- DACs also independent
- In measurement:
  - Used one universal DAC code
  - Conclusion: the stage-to-stage variation in signal independent overshoot is small enough for a single global control

Overshoot Cancellation (C_{DAC})

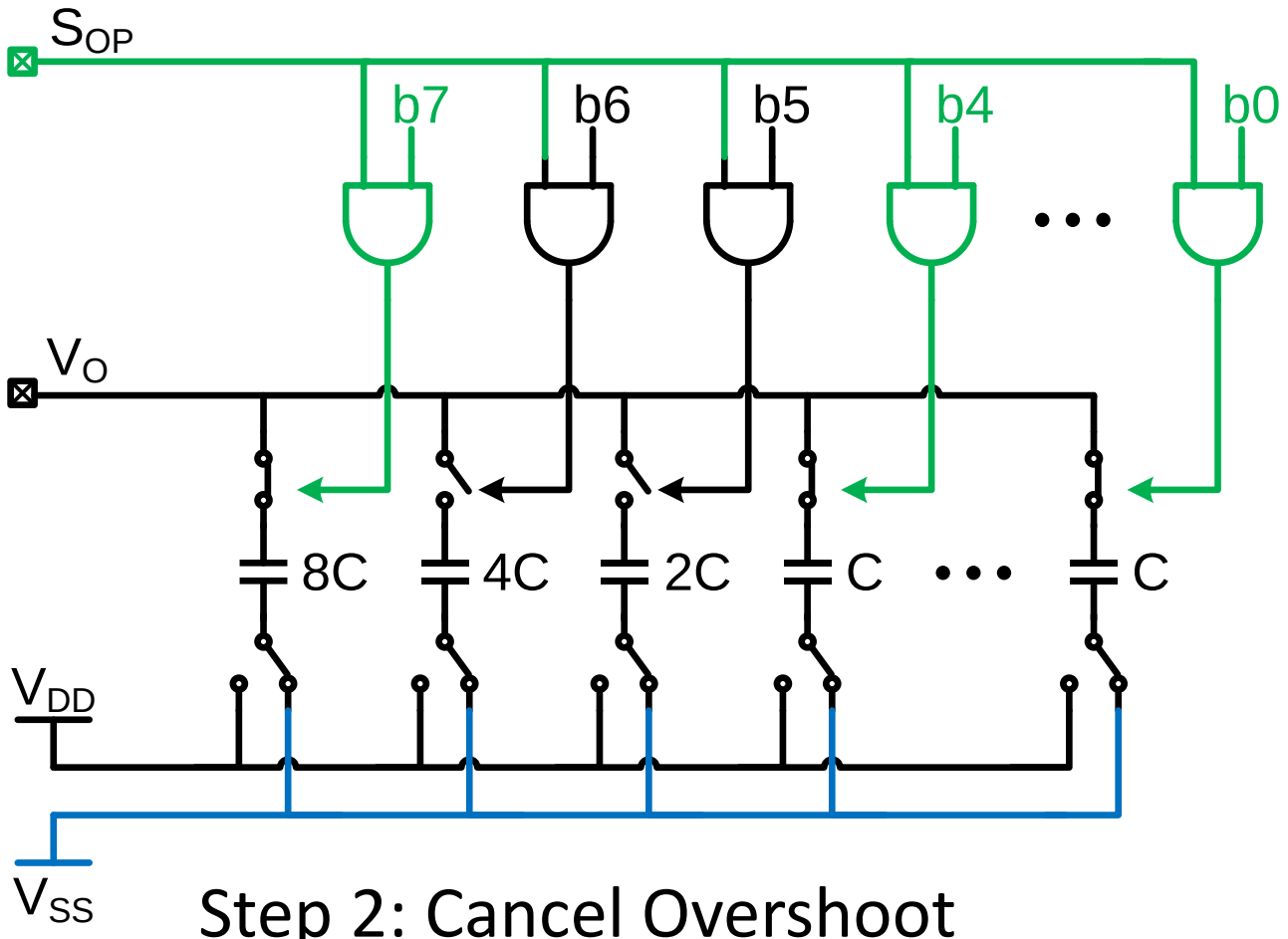


Overshoot Cancellation (C_{DAC})



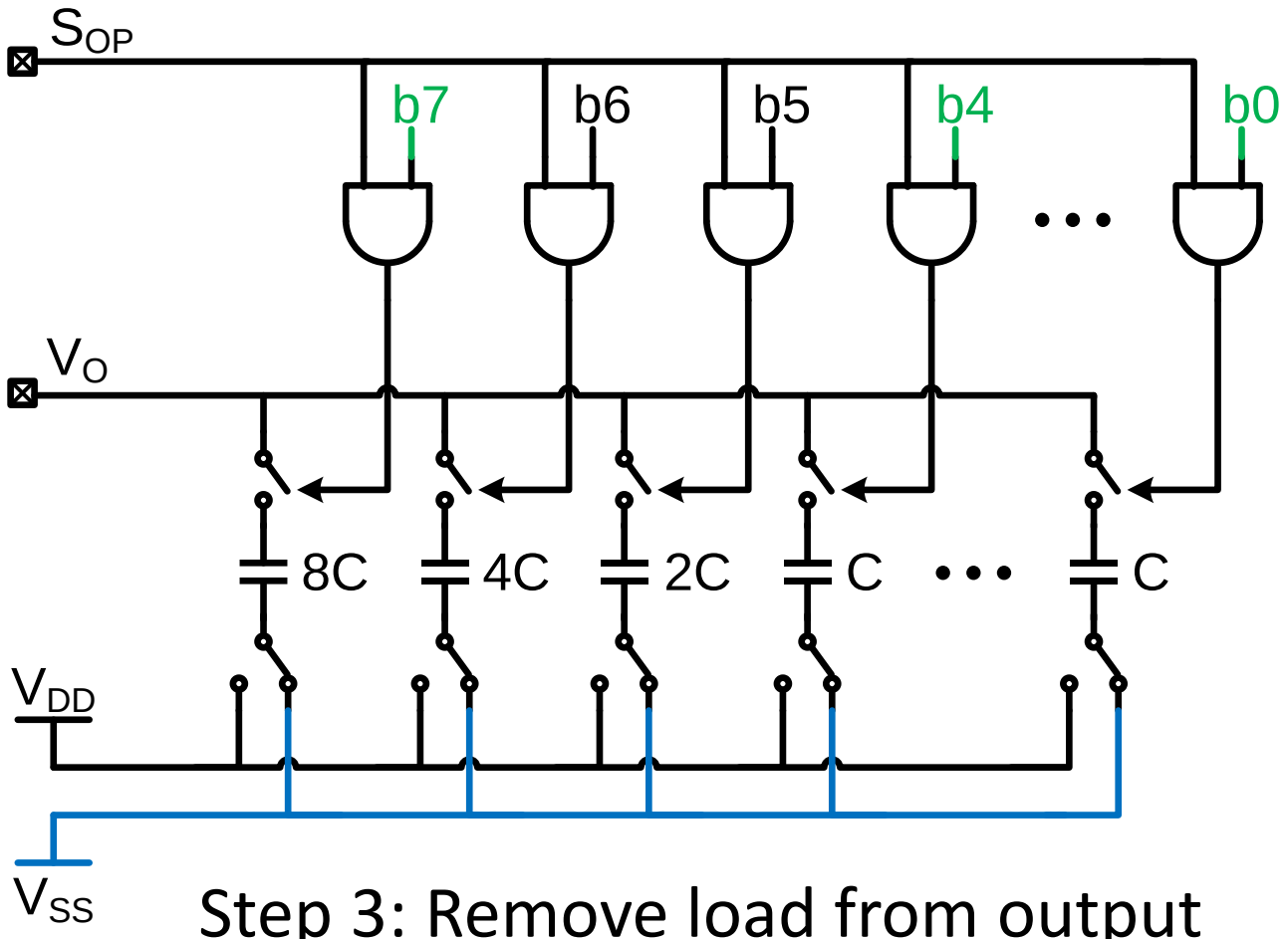
Step 1: Track ZCBC waveform

Overshoot Cancellation (C_{DAC})



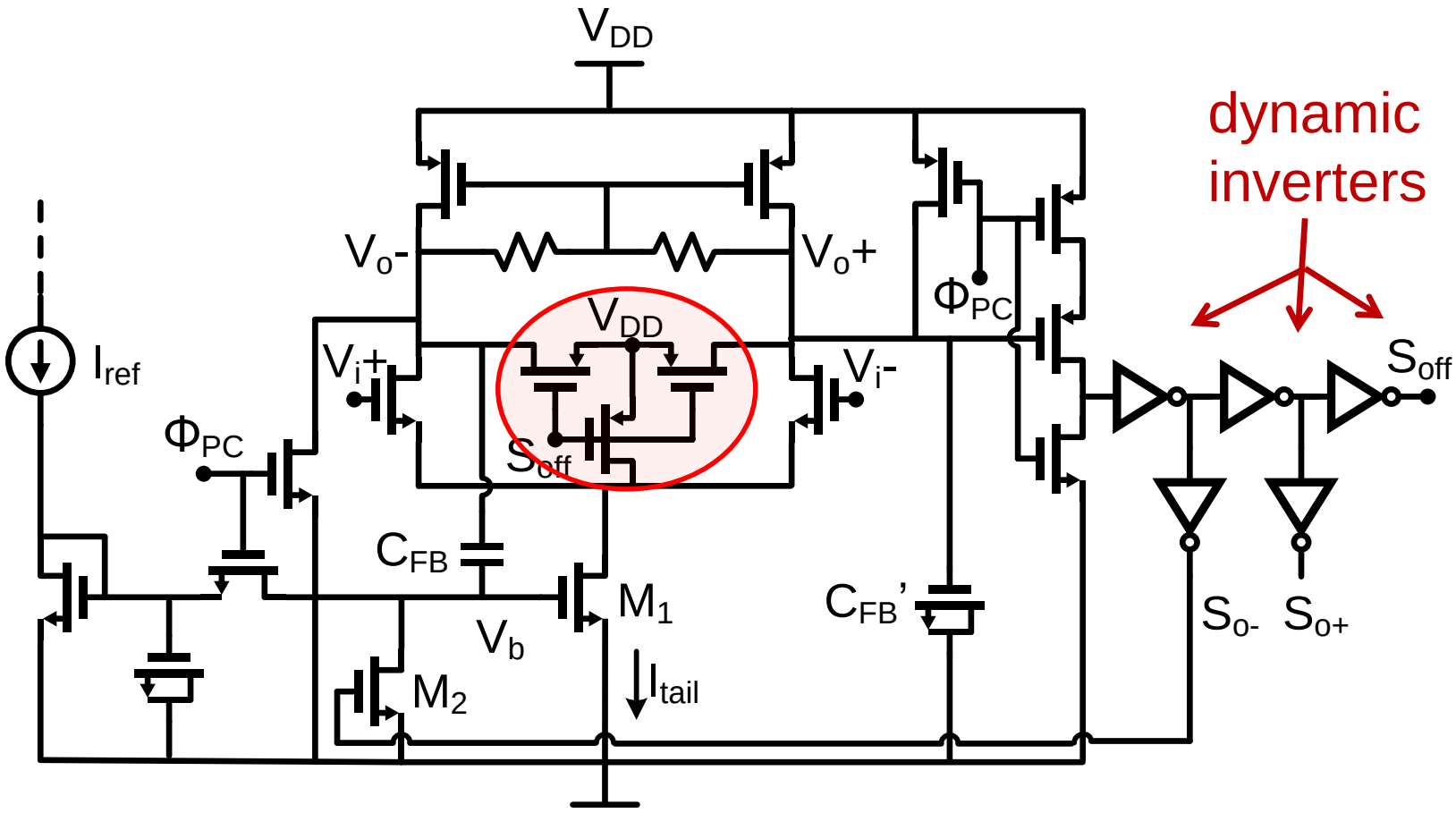
Step 2: Cancel Overshoot

Overshoot Cancellation (C_{DAC})



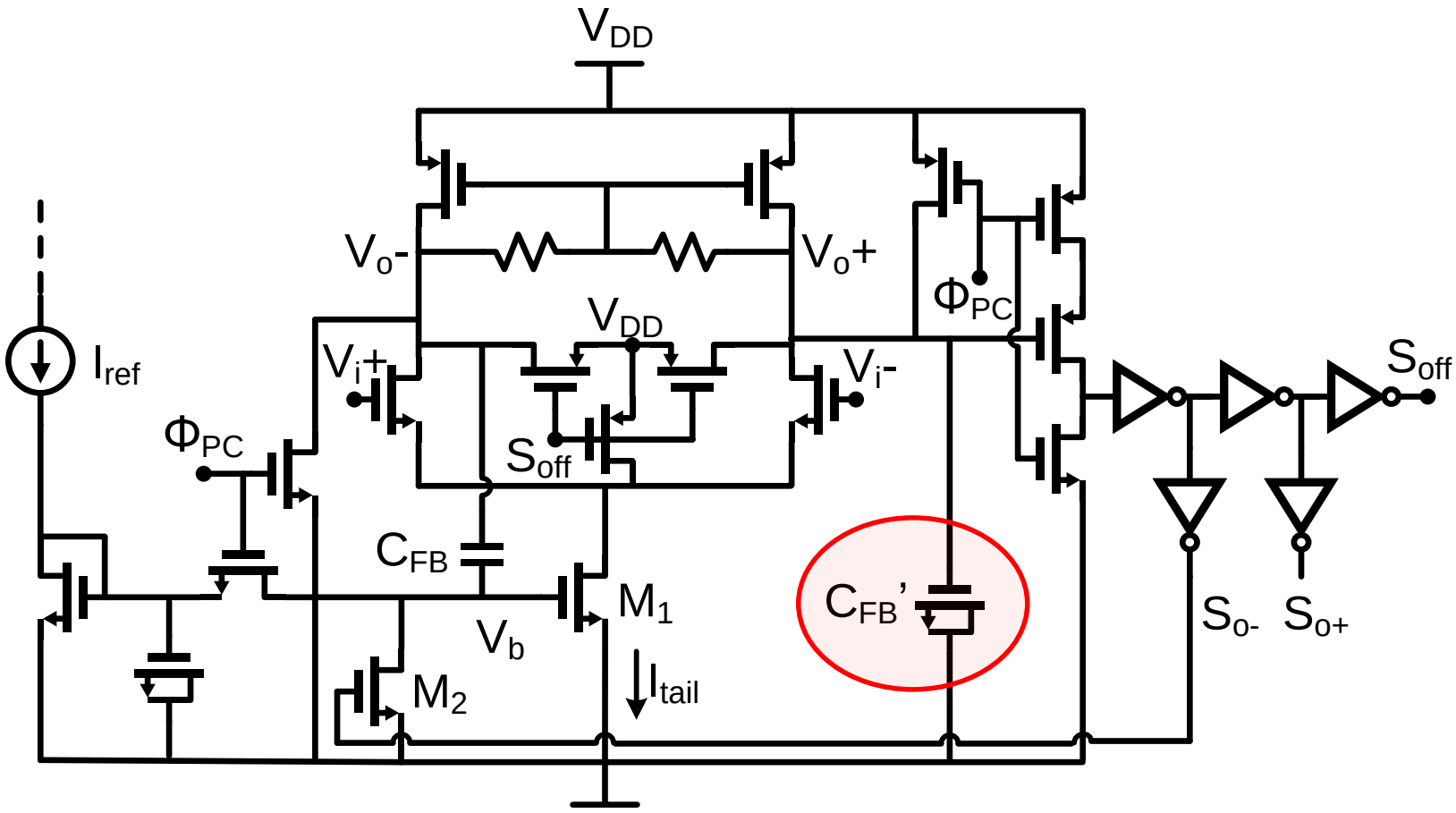
Step 3: Remove load from output

Dynamic ZCD (detail)



Reset switches to reset kickback charge

Dynamic ZCD (detail)

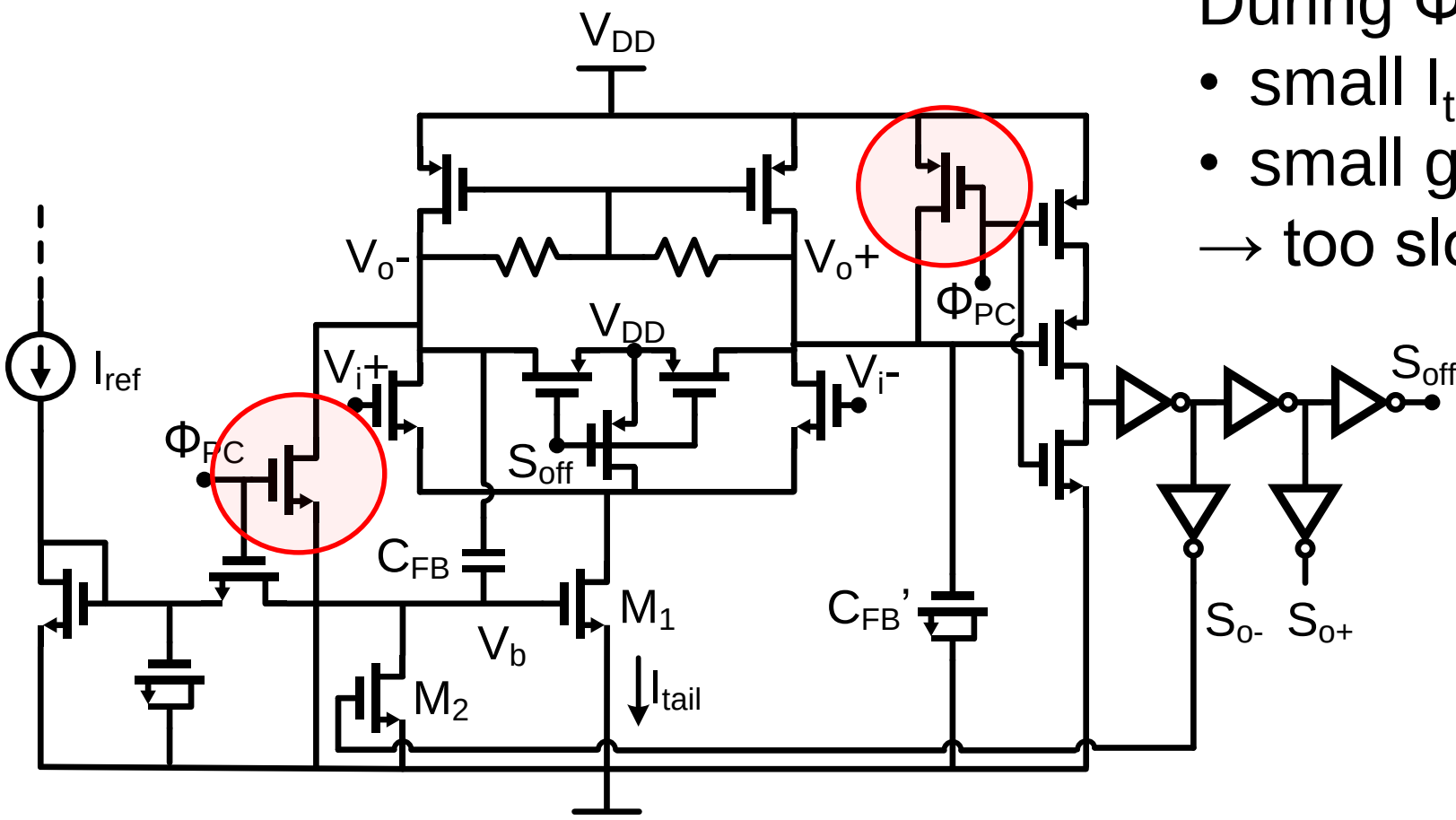


Dummy load to match Vo+ load with Vo-

Dynamic ZCD (detail)

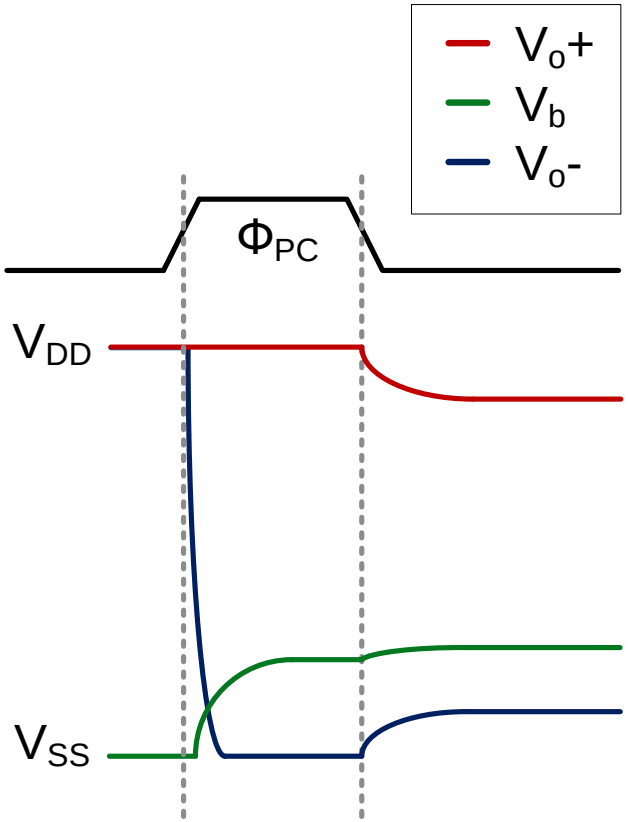
During Φ_{PC}:
- small I_{tail}
- small g_m

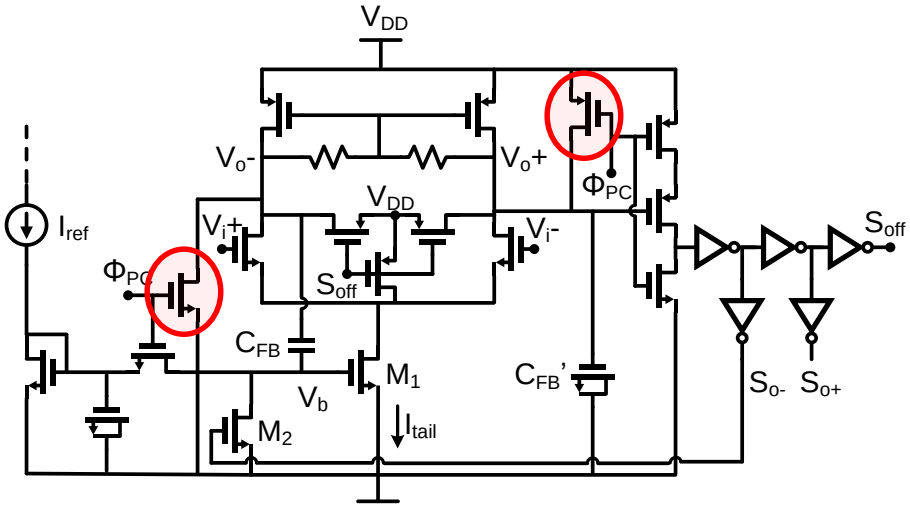
→ too slow!



Pre-charge switches

Dynamic ZCD (detail)





- Theoretically possible to guarantee $I_{tail} > 0$ for *any* bias input

Pre-charge switches